

**AK2365****dPMR Filterless IF LSI**

## 1. Features

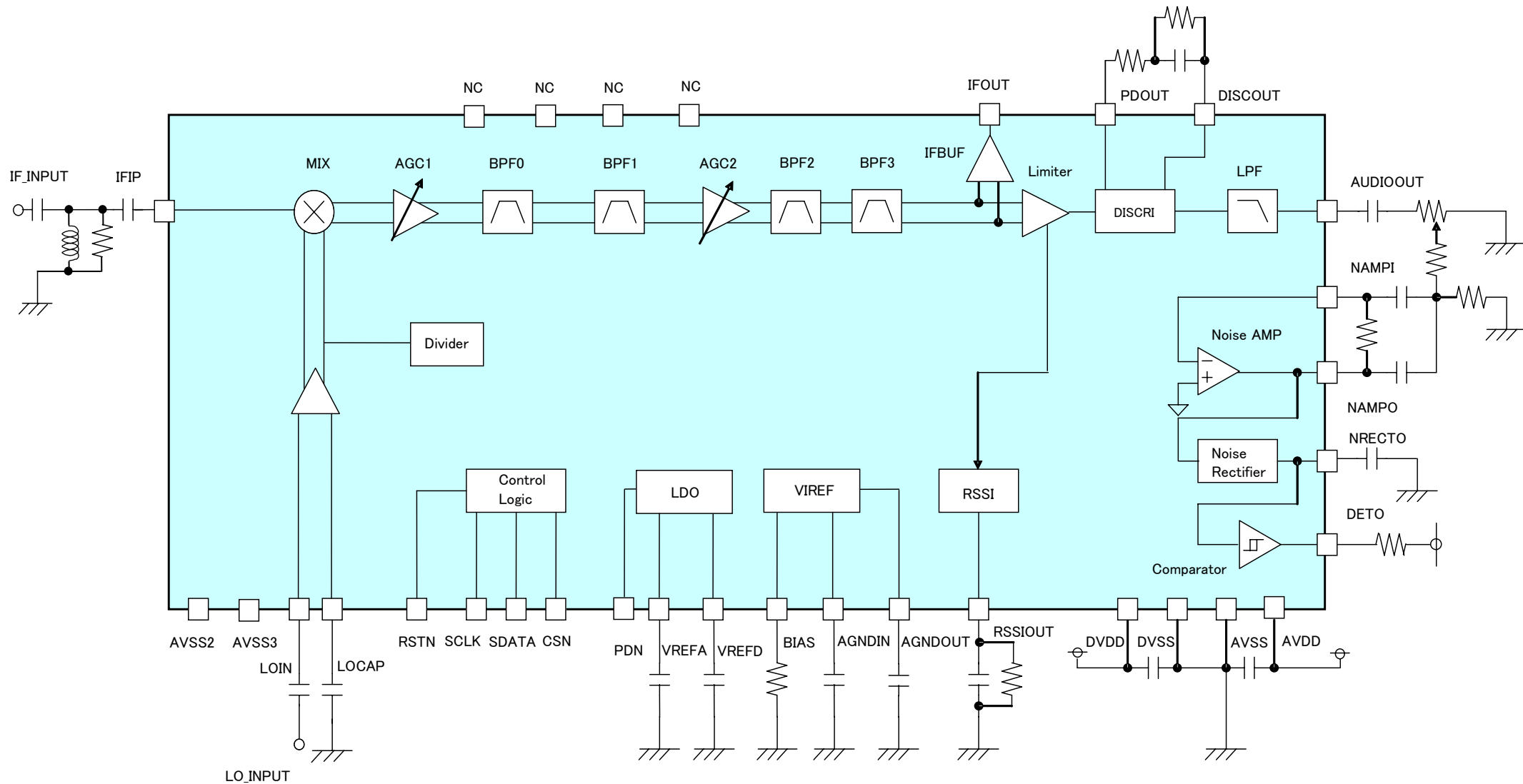
The AK2365 includes 2nd-Mixer, AGC+BPF, PLL FM detector, noise squelch, and RSSI circuit. This device can eliminate E to J type ceramic filters, quadrature discriminator, and other external components.

- Low operating voltage:  $V_{DD} = 2.6$  to  $5.5$  V
- Wide operating temperature:  $T_a = -40$  to  $85$  °C
- High sensitivity:  $-102$ dBm at 12dB SINAD
- Built-in PGA and 2nd Mixer
- Local frequency: 45.9MHz, 50.4MHz, 57.6MHz (Triple of 15.3, 16.8 and 19.2MHz)
- Built-in programmable AGC+BPF circuits corresponding to E to J type ceramic filters
- Built-in PLL FM detector
- RSSI function
- Built-in noise squelch circuits
- Low consumption current: 6mA
- Compact plastic packaging: 32-pin QFNJ (4.0 x 4.0 x 0.75mm, 0.4mm pitch)

|                    |
|--------------------|
| <b>2. Contents</b> |
|--------------------|

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### 3. Block Diagram



## 4. Circuit Configuration

| Block           | Description                                                                                                                                                  |
|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MIX             | 2nd-mixer to convert the input signal down to 450kHz.                                                                                                        |
| AGC+BPF         | The circuit composed of AGC and BPF, where the desired signal is amplified and spurious components included in the signal from the 2nd-mixer are eliminated. |
| IFBUF           | The circuit to output filtered signal by AGC+BPF.                                                                                                            |
| Divider         | The circuit to divide the signal from LOIN pin.                                                                                                              |
| Limiter         | The circuit to amplify the signal filtered at the AGC+BPF stage and generate rectangular wave.                                                               |
| DISCRI          | The demodulator circuit with PLL FM detector, where the audio signal is recovered.                                                                           |
| LPF             | The Low-pass filter to eliminate the noise generated at the DISCRI stage.                                                                                    |
| Noise AMP       | The amplifiers to compose the Band-pass filter for noise squelch.                                                                                            |
| Noise Rectifier | The rectification circuit to detect the noise level.                                                                                                         |
| Comparator      | The circuit to compare the noise level with reference voltage level.                                                                                         |
| RSSI            | The circuit to indicate the Received Signal Strength Indicator (RSSI) by generating a DC voltage corresponding to the input level from Limiter.              |
| VIREF           | The circuit to generate internal reference voltage.                                                                                                          |
| LDO             | The circuit to supply 2.7V power for some circuits.                                                                                                          |
| Control Logic   | The control register controls the status of internal condition by serial data that consists of 1 instruction bit, 6 address bits and 8 data bits.            |

## 5. Pin/Function

| Package | Signal   |      |                          | Function                                                                                 |
|---------|----------|------|--------------------------|------------------------------------------------------------------------------------------|
| Pin No  | Name     | Type | Conditions at power down |                                                                                          |
| 1       | IFIP     | AI   | Note 1)                  | IF signal input pin                                                                      |
| 2       | NC       | AIO  | Z                        | NC pin                                                                                   |
| 3       | NC       | AIO  | Z                        | NC pin                                                                                   |
| 4       | NC       | AIO  | Z                        | NC pin                                                                                   |
| 5       | NC       | AIO  | Z                        | NC pin                                                                                   |
| 6       | VREFA    | AO   | Low                      | LDO reference pin<br>Connect the capacitor to stabilize LDO reference voltage.           |
| 7       | AVSS     | PWR  | -                        | Analog VSS power supply pin                                                              |
| 8       | AVDD     | PWR  | -                        | Analog VDD power supply pin                                                              |
| 9       | BIAS     | AO   | Z                        | Output pin to connect bias resistor for reference voltage                                |
| 10      | NRECTO   | AI   | Note 2)                  | Output pin for the rectification circuit                                                 |
| 11      | NAMPO    | AO   | Z                        | Output pin for noise squelch amplifier                                                   |
| 12      | NAMPI    | AI   | Z                        | Input pin for noise squelch amplifier                                                    |
| 13      | AUDIOOUT | AO   | Note 3)                  | Demodulated audio signal output pin                                                      |
| 14      | DISCOUT  | AO   | Note 4)                  | Pin2 for Discriminator Low-pass filter                                                   |
| 15      | PDOUT    | AO   | Z                        | Pin1 for Discriminator Low-pass filter                                                   |
| 16      | RSSIOUT  | AO   | Z                        | Output pin to connect capacitor for Received Signal Strength Indicator(RSSI)             |
| 17      | IFOUT    | AO   | Note 5)                  | Output pin for IFBUF                                                                     |
| 18      | AVSS2    | PWR  | -                        | Analog VSS power supply pin                                                              |
| 19      | PDN      | DI   | Z                        | Power down pin for LDO                                                                   |
| 20      | RSTN     | DI   | Z                        | Hardware reset pin                                                                       |
| 21      | CSN      | DI   | Z                        | Chip select input pin for serial data                                                    |
| 22      | SCLK     | DI   | Z                        | Clock input pin for serial data                                                          |
| 23      | SDATA    | DB   | Z                        | Input and output pin for serial data                                                     |
| 24      | DETO     | DO   | Z                        | Signal detect output pin                                                                 |
| 25      | DVDD     | PWR  | -                        | Digital VDD power supply pin.                                                            |
| 26      | DVSS     | PWR  | -                        | Digital VSS power supply pin.                                                            |
| 27      | VREFD    | AO   | Low                      | LDO reference pin<br>Connect the capacitor to stabilize LDO reference voltage.           |
| 28      | AVSS3    | PWR  | -                        | Analog VSS power supply pin                                                              |
| 29      | AGNDOUT  | AO   | Low                      | Analog ground output pin.<br>Connect the capacitor to stabilize the analog ground level. |
| 30      | AGNDIN   | AI   | Low                      | Analog ground input pin.<br>Connect the capacitor to stabilize the analog ground level.  |
| 31      | LOCAP    | AI   | Note 6)                  | Local signal input pin                                                                   |
| 32      | LOIN     | AI   | Note 6)                  | Local signal input pin                                                                   |

Note A: Analog, D: Digital, PWR: Power, I: Input, O: Output, B: Bidirectional, Z: High-Z, L: Low

Note 1) Connecting internally to VSS pin by 50kΩ

Note 2) Connecting internally to VDD pin by 720kΩ

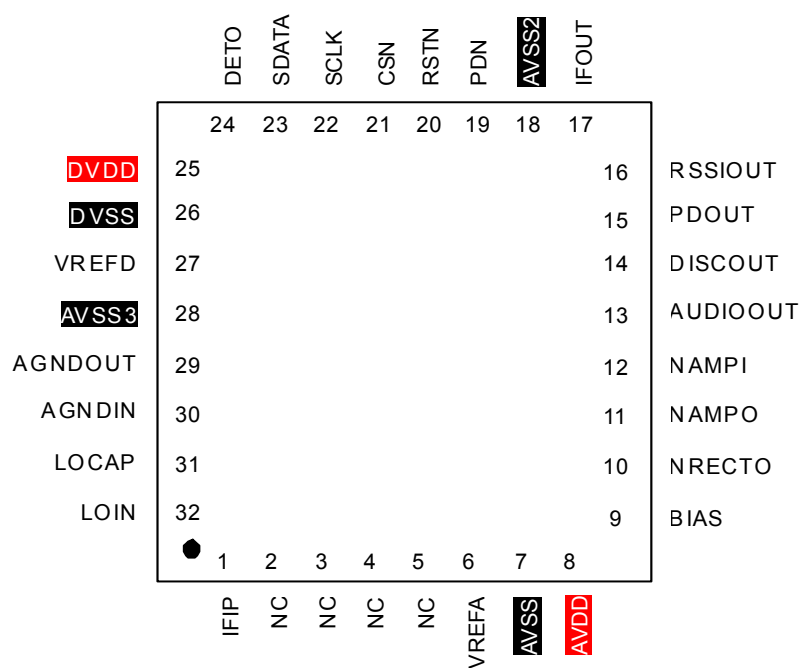
Note 3) Connecting internally to VSS pin by 830kΩ

Note 4) Connecting internally to VSS pin by 50k $\Omega$

Note 5) Connecting internally to VSS pin by 480k $\Omega$

Note 5) Connecting internally to VDD pin by 139k $\Omega$

• Pin Assignment



## 6. Absolute Maximum Ratings

| Parameter                                  | Symbol                  | Min. | Max.     | Units |
|--------------------------------------------|-------------------------|------|----------|-------|
| Power Supply Voltage                       | AVDD                    | -0.3 | 6.5      | V     |
|                                            | DVDD                    | -0.3 | 6.5      | V     |
| Ground Level                               | VSS                     | 0    | 0        | V     |
| Input Voltage                              | V <sub>IN</sub> analog  | -0.3 | AVDD+0.3 | V     |
|                                            | V <sub>IN</sub> digital | -0.3 | DVDD+0.3 | V     |
| Input Current<br>(Except power supply pin) | I <sub>IN</sub>         | -10  | +10      | mA    |
| Storage Temperature                        | T <sub>stg</sub>        | -55  | 125      | °C    |

Note : All voltages are relative to the VSS pin.

Caution : Exceeding these maximum ratings can result in damage to the device.  
Normal operation cannot be guaranteed under this extreme.

## 7. Recommended Operating Conditions

| Parameter                | Symbol          | Condition                    | Min. | Typ.         | Max. | Units |
|--------------------------|-----------------|------------------------------|------|--------------|------|-------|
| Operating Temperature    | Ta              |                              | -40  |              | 85   | °C    |
| Power Supply Voltage     | AVDD            |                              | 2.6  | 3.0          | 5.5  | V     |
|                          | DVDD            | DVDD ≤ AVDD                  | 2.6  | 3.0          | 5.5  | V     |
| Analog Reference Voltage | AGND            | AGNDOUT                      |      | 1/2<br>VREFA |      | V     |
| Output Load Resistance   | R <sub>L1</sub> | AUDIOOUT, DISCOUNT,<br>NAMPO | 30   |              |      | kΩ    |
| Output Load Capacitance  | C <sub>L1</sub> | AUDIOOUT, DISCOUNT,<br>NAMPO |      |              | 15   | pF    |
|                          | C <sub>L2</sub> | IFOUT                        |      | 21           | 26   | pF    |

Note : All voltages are relative to the VSS pin.

|                               |
|-------------------------------|
| 8. Digital DC Characteristics |
|-------------------------------|

| Parameter                 | Symbol   | Condition                                       | Min.     | Typ. | Max.    | Units   |
|---------------------------|----------|-------------------------------------------------|----------|------|---------|---------|
| High level input voltage  | $V_{IH}$ | RSTN, SCLK, SDATA,<br>CSN, PDN                  | 0.8DVDD  |      |         | V       |
| Low level input voltage   | $V_{IL}$ | RSTN, SCLK, SDATA,<br>CSN, PDN                  |          |      | 0.2DVDD | V       |
| High level input current  | $I_{IH}$ | $V_{IH}=DVDD$<br>RSTN, SCLK, SDATA,<br>CSN, PDN |          |      | 10      | $\mu A$ |
| Low level input current   | $I_{IL}$ | $V_{IL}=0V$<br>RSTN, SCLK, SDATA,<br>CSN, PDN   | -10      |      |         | $\mu A$ |
| High level output voltage | $V_{OH}$ | $I_{OH}=+0.2mA$<br>SDATA                        | DVDD-0.4 |      | DVDD    | V       |
| Low level output voltage  | $V_{OL}$ | $I_{OL}=-0.4mA$<br>SDATA, DETO                  | 0.0      |      | 0.4     | V       |

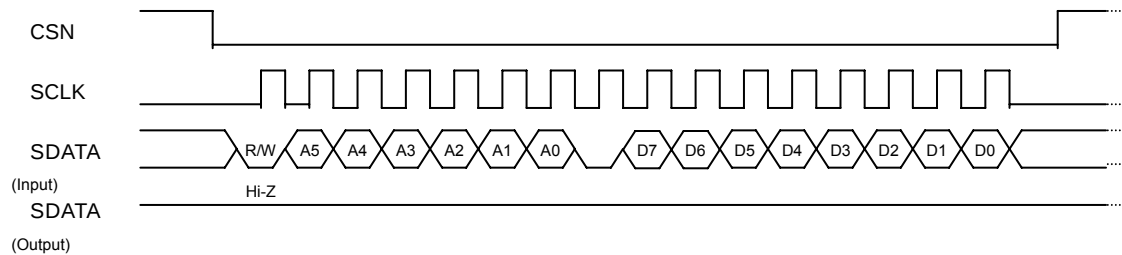
## 9. Digital AC Timing

### 1) Serial Interface Timing

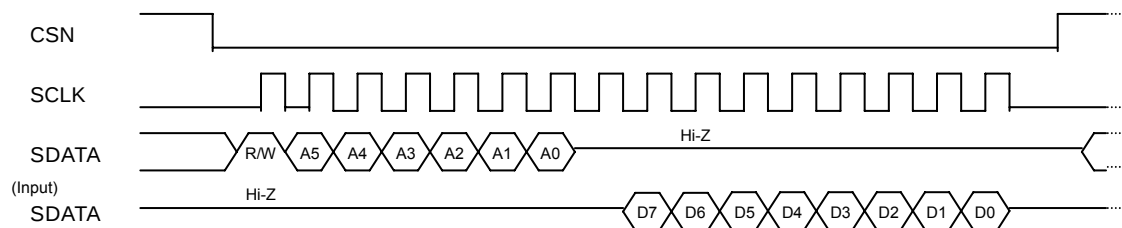
AK2365 is connected to a CPU by three-wired interface through CSN, SCLK and SDATA pins, which can make reading and writing data for control registers.

Serial data named SDATA is consist of 1-bit read and write instruction(R/W), 6-bit address (A5 to A0) and 8-bit data(D7 to D0) in one frame.

#### Write mode



#### Read mode



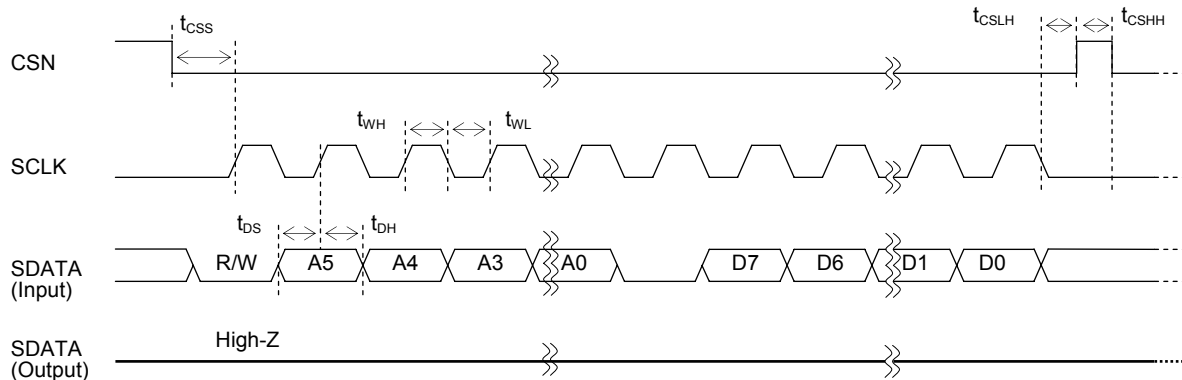
R/W : Instruction bit controls to write data to AK2365 or read back from it.  
When set to low, AK2365 is in write mode. When set to high, AK2365 is in read mode.

A5 to A0: Register address to be accessed.  
D7 to D0: Write or read data to be accessed.

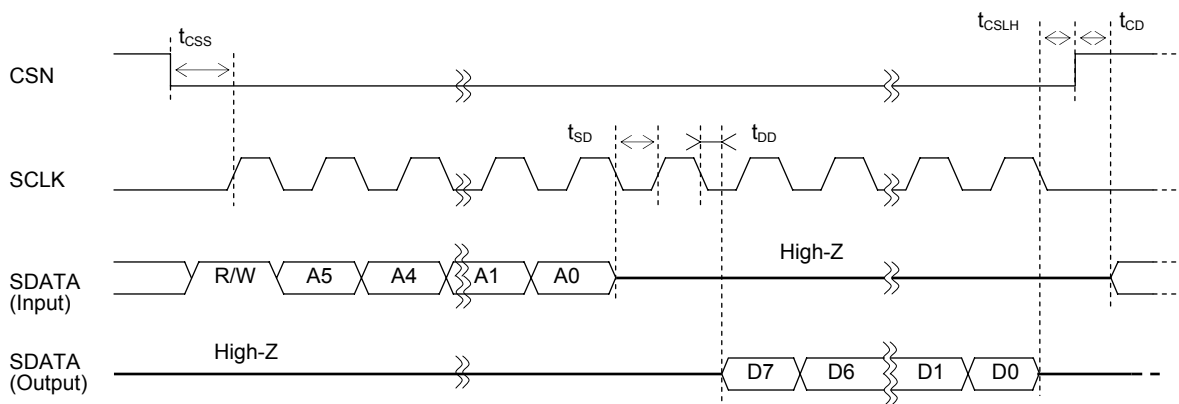
- <1> CSN(Chip select) is normally selected high for disable.  
When CSN is set to low, serial interface becomes active.
- <2> In write mode, instruction, address and data input from SDATA pin are synchronized and latched with the rising edge of 16 iterations of SCLK clock. Set to low between address A0 and data D7. Input data is fixed synchronized with the rising edge of 16th clock. Note that if CSN become "H" before 16th clock, setting data becomes invalid. During the period when CSN is set to "L", consecutive writing is available.
- <3> In read mode, instruction and address are synchronized and latched with the rising edge of 7 iterations of SCLK clock. And the register data are output from SDATA pin synchronized with the falling edge of 9 iterations of SCLK clock. The data between address A0 and data D7 is unstable. During the period when data is output, input to SDATA must be "Hi-z". Set CSN to "H" once reading is completed because consecutive reading is not valid.

## 2) Detail Timing Chart

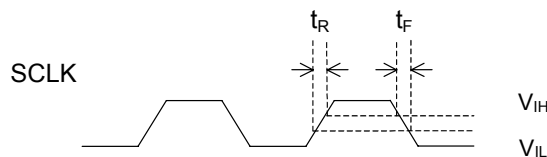
## Write mode



## Read mode



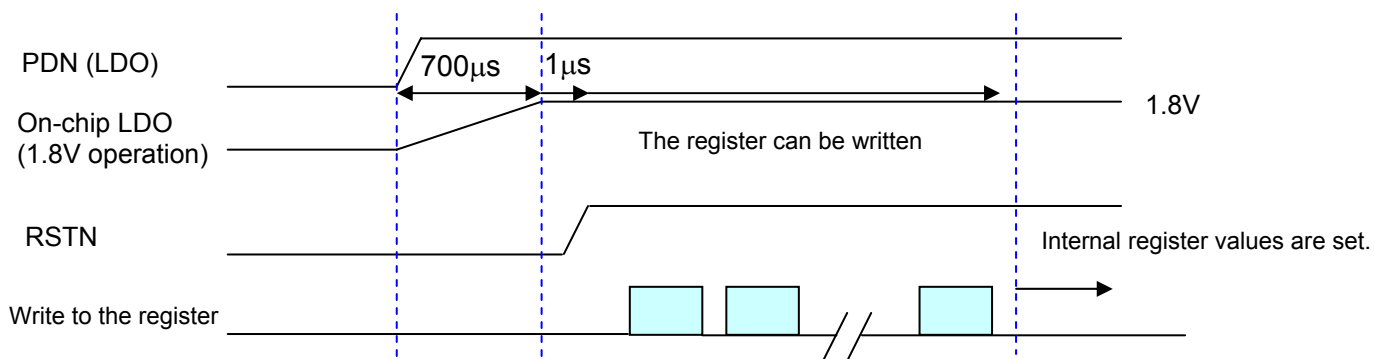
## Rising and falling time



| Parameter                       | Symbol     | Condition | Min. | Typ. | Max. | Unit |
|---------------------------------|------------|-----------|------|------|------|------|
| CSN setup time                  | $t_{CSS}$  |           | 100  |      |      | ns   |
| SDATA setup time                | $t_{DS}$   |           | 100  |      |      | ns   |
| SDATA hold time                 | $t_{DH}$   |           | 100  |      |      | ns   |
| SCLK high time                  | $t_{WH}$   |           | 500  |      |      | ns   |
| SCLK low time                   | $t_{WL}$   |           | 500  |      |      | ns   |
| CSN low hold time               | $t_{CSLH}$ |           | 100  |      |      | ns   |
| CSN high hold time              | $t_{CSHH}$ |           | 100  |      |      | ns   |
| SDATA Hi-Z setup time           | $t_{SD}$   |           | 500  |      |      | ns   |
| SCLK to SDATA output delay time | $t_{DD}$   | 20pF load |      |      | 400  | ns   |
| CSN to SDATA input delay time   | $t_{CD}$   | 20pF load | 200  |      |      | ns   |
| SCLK rising time                | $t_R$      |           |      |      | 250  | ns   |
| SCLK falling time               | $t_F$      |           |      |      | 250  | ns   |

Note) Digital input and output timing is relative to 0.5DVDD of rising signal and falling signal.

## 10. Power-up Sequence

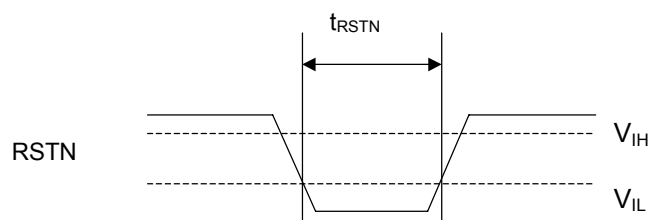


Note) After PDN is set to “High”, registers remain undefined. In order to initialize them, RSTN is set to “High”

## 11. System Reset

| Parameter                         | Symbol     | Condition     | Min. | Typ. | Max. | Unit | Remarks |
|-----------------------------------|------------|---------------|------|------|------|------|---------|
| Hardware reset signal input width | $t_{RSTN}$ | RSTN pin      | 1    |      |      | µs   | *1)     |
| Software reset                    |            | SRST register |      |      |      |      | *2)     |

\*1) After power-on, be sure to perform a hardware reset operation (register initialization). The system is reset by a low pulse input of 1µs (min.) and enters the normal operation state. At this moment, the digital (DI) pins are set as follows: RSTN pin to High, SCLK pin to Low, SDATA pin to Low, CSN pin to Low.



\*2) When data 0x04:10101010 is written to the SRST[7:0] register, software reset is performed. This setting initializes the registers and the operation mode is set to mode 2 (Standby 2). After software reset is completed, this register comes to “0”.

|                       |
|-----------------------|
| 12. Power Consumption |
|-----------------------|

| Parameter         | Symbol | Condition                                     | Min. | Typ. | Max. | Units |
|-------------------|--------|-----------------------------------------------|------|------|------|-------|
| Power Consumption | IDD0   | Mode 0<br>Power down                          |      |      | 0.01 | mA    |
|                   | IDD1   | Mode 1<br>Standby 1                           |      | 0.3  | 0.6  |       |
|                   | IDD2   | Mode 2<br>Standby 2                           |      | 0.4  | 0.7  |       |
|                   | IDD3   | Mode 3                                        |      | 1    | 1.6  |       |
|                   | IDD4   | Mode 4<br>Digital Mode 1 with no signal input |      | 5.6  | 7.5  |       |
|                   | IDD5   | Mode 5<br>Digital Mode 2 with no signal input |      | 6    | 8    |       |
|                   | IDD6   | Mode 6<br>Analog Mode with no signal input    |      | 6    | 8    |       |
|                   | IDD7   | Mode 7<br>Full Power On with no signal input  |      | 7    | 9.8  |       |

### 13. Analog Characteristics

For the following conditions unless otherwise specified: Mode 6, LOIN=50.4MHz, IFIP=50.85MHz,  $\Delta f = \pm 1.5\text{kHz}$ ,  $f_{\text{mod}} = 1\text{kHz}$ , AGC+BPF=F2, {AGC\_OFF}=0, the exposure back pad of the package is connected to VSS, with the external circuit shown in example page 26 to 28.

#### 1) Local

| Parameter       | Symbol          | Condition | Min. | Typ.                 | Max. | Units           | Notes   |
|-----------------|-----------------|-----------|------|----------------------|------|-----------------|---------|
| Local Frequency | $F_{\text{LO}}$ | LOIN      |      | 45.9<br>50.4<br>57.6 |      | MHz             |         |
| Input amplitude | $V_{\text{LO}}$ | LOIN      | 0.2  |                      | 2.0  | $V_{\text{PP}}$ | Note 1) |

Note 1) Input from LOIN pin through DC cut

#### 2) 2nd Mixer

| Parameter       | Condition | Min. | Typ.                     | Max. | Units    | Notes   |
|-----------------|-----------|------|--------------------------|------|----------|---------|
| Input Impedance |           |      | 50                       |      | $\Omega$ | Note 2) |
| Input Frequency |           |      | $F_{\text{LO}}$<br>+0.45 |      | MHz      |         |
| Voltage Gain    |           |      | 28                       |      | dB       |         |

Note 2) Include external matching circuit

#### 3) Discriminator

| Parameter                 | Condition                                                                                                                                  | Min. | Typ. | Max. | Units | Notes   |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|---------|
| Demodulation Output Level | $\Delta f = \pm 3.0\text{kHz}$ , $f_{\text{mod}} = 1\text{kHz}$ ,<br>LIMITER IN to AUDIOOUT<br>{BAND}=1                                    | 70   | 100  | 130  | mVrms |         |
|                           | $\Delta f = \pm 1.5\text{kHz}$ , $f_{\text{mod}} = 1\text{kHz}$ ,<br>LIMITER IN to AUDIOOUT<br>{BAND}=0                                    | 70   | 100  | 130  | mVrms |         |
| S/N Ratio                 | $\Delta f = \pm 3.0\text{kHz}$ , $f_{\text{mod}} = 1\text{kHz}$ ,<br>$V_{\text{in}} = -16\text{dBm}$<br>LIMITER IN to AUDIOOUT<br>{BAND}=1 | 43   | 50   |      | dB    | Note 3) |

Note 3) With De-emphasis + BPF(0.3 to 3kHz)

## 4) RX Overall Characteristics

| Parameter                       | Condition                                                                                                                    | Min. | Typ. | Max. | Units | Notes   |
|---------------------------------|------------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|---------|
| 12dB SINAD<br>Input Sensitivity |                                                                                                                              |      | -102 |      | dBm   | Note 4) |
| Total Gain                      | Mode 5<br>Maximum gain setting for AGC<br>IFIP to IFOUT<br>{IFOG[1:0]}=00                                                    |      | 84   |      | dB    |         |
|                                 | Mode 5<br>Minimum gain setting for AGC<br>IFIP to IFOUT<br>{IFOG[1:0]}=00                                                    |      | 32   |      | dB    |         |
| C/N ratio                       | Mode 5, BPF=F3<br>IFIP to IFOUT<br>When in CW, 450kHz, -102dBm<br>Bandwidth: 450kHz $\pm$ 3kHz<br>{IFOG[1:0]}=00             |      | 17   |      |       |         |
| IIP3                            | Mode 5<br>Maximum gain setting for AGC<br>IFIP=50.8635MHz&50.876MHz                                                          |      | -20  |      | dBm   |         |
| Demodulation<br>Output<br>Level | $\Delta f = \pm 3.0\text{kHz}$ , $f_{\text{mod}} = 1\text{kHz}$ ,<br>AGC+BPF=F1, {BAND}=1                                    | 70   | 100  | 130  | mVrms |         |
|                                 | $\Delta f = \pm 1.5\text{kHz}$ , $f_{\text{mod}} = 1\text{kHz}$ ,<br>AGC+BPF=F2, {BAND}=0                                    | 70   | 100  | 130  | mVrms |         |
| S/N Ratio                       | $\Delta f = \pm 3.0\text{kHz}$ , $f_{\text{mod}} = 1\text{kHz}$ ,<br>AGC+BPF=F1, $V_{\text{in}} = -47\text{dBm}$<br>{BAND}=1 | 40   | 50   |      | dB    | Note 4) |
|                                 | $\Delta f = \pm 1.5\text{kHz}$ , $f_{\text{mod}} = 1\text{kHz}$ ,<br>AGC+BPF=F2, $V_{\text{in}} = -47\text{dBm}$<br>{BAND}=0 | 34   | 44   |      | dB    | Note 4) |

Note 4) With De-emphasis+BPF(0.3 to 3kHz)

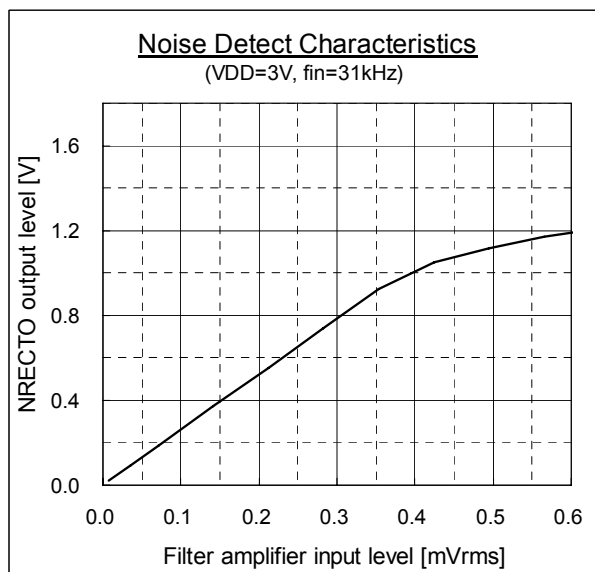
## 5) RSSI Characteristics

| Parameter           | Condition                                             | Min. | Typ. | Max. | Units | Notes |
|---------------------|-------------------------------------------------------|------|------|------|-------|-------|
| RSSI Output Voltage | IFIP to RSSIOUT<br>{AGC_OFF}=0,<br>IFIP=-100dBm Input | 0.05 | 0.3  | 0.7  | V     |       |
|                     | IFIP to RSSIOUT<br>{AGC_OFF}=0,<br>IFIP=-30dBm Input  | 1.4  | 2.0  | 2.6  | V     |       |



## 6) Noise Squelch Characteristics

| Parameter                      | Condition                                  | Min. | Typ. | Max. | Units | Notes |
|--------------------------------|--------------------------------------------|------|------|------|-------|-------|
| Noise Detection Level          | NRECTO to DETO<br>Detect High              |      | 0.5  | 0.7  | V     |       |
|                                | NRECTO to DETO<br>Detect Low               | 0.3  | 0.4  |      | V     |       |
| Noise Detection Characteristic | NAMPI to NRECTO<br>Input: 31kHz, 0.1mVrms  | 0.2  | 0.3  | 0.4  | V     |       |
|                                | NAMPI to NRECTO<br>Input: 31kHz, 0.25mVrms | 0.5  | 0.65 | 0.8  | V     |       |



## 7) AGC+BPF Characteristics

## 7.1) F0 (E type)

| Parameter                                                       | Condition       | Min. | Typ. | Max. | Units | Notes |
|-----------------------------------------------------------------|-----------------|------|------|------|-------|-------|
| Attenuation Characteristics<br>(relative to the gain at 450kHz) | 435kHz          |      |      | -50  | dB    |       |
|                                                                 | 442.5kHz        | -6   |      |      | dB    |       |
|                                                                 | 457.5kHz        | -6   |      |      | dB    |       |
|                                                                 | 465kHz          |      |      | -50  | dB    |       |
| Gain ripple                                                     | Within 450±5kHz |      |      | 3    | dB    |       |

## 7.2) F1 (F type)

| Parameter                                                       | Condition       | Min. | Typ. | Max. | Units | Notes |
|-----------------------------------------------------------------|-----------------|------|------|------|-------|-------|
| Attenuation Characteristics<br>(relative to the gain at 450kHz) | 437.5kHz        |      |      | -50  | dB    |       |
|                                                                 | 444kHz          | -6   |      |      | dB    |       |
|                                                                 | 456kHz          | -6   |      |      | dB    |       |
|                                                                 | 462.5kHz        |      |      | -50  | dB    |       |
| Gain ripple                                                     | Within 450±4kHz |      |      | 3    | dB    |       |

## 7.3) F2 (G type)

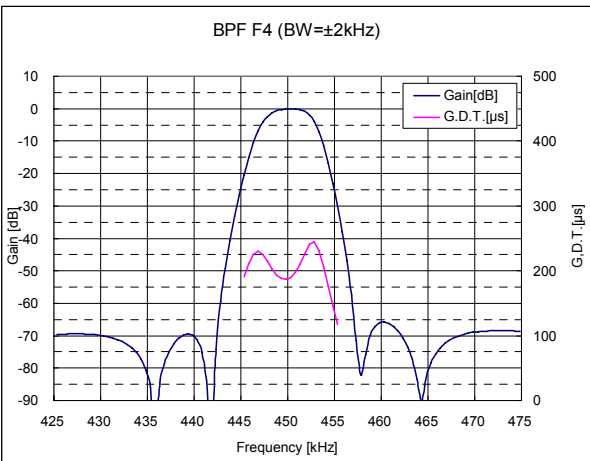
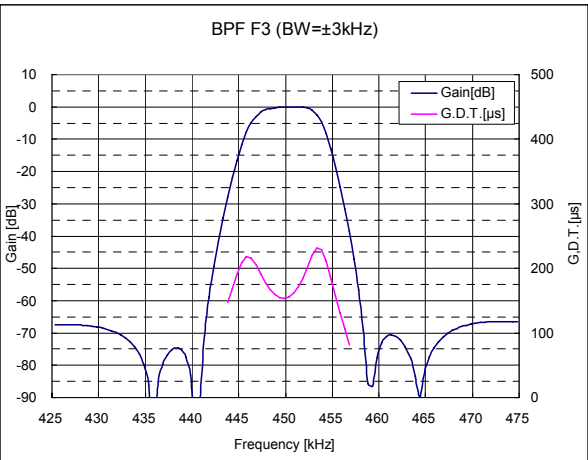
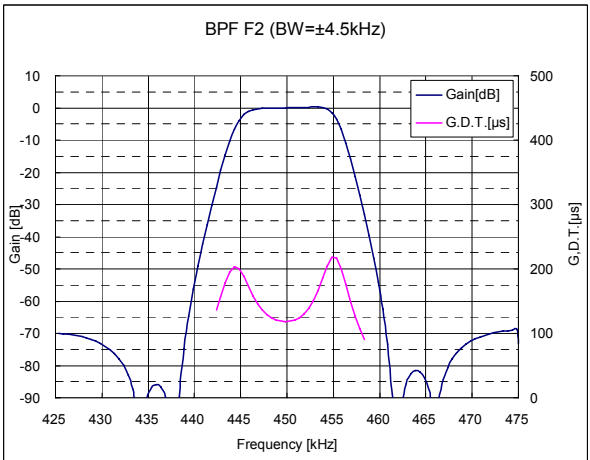
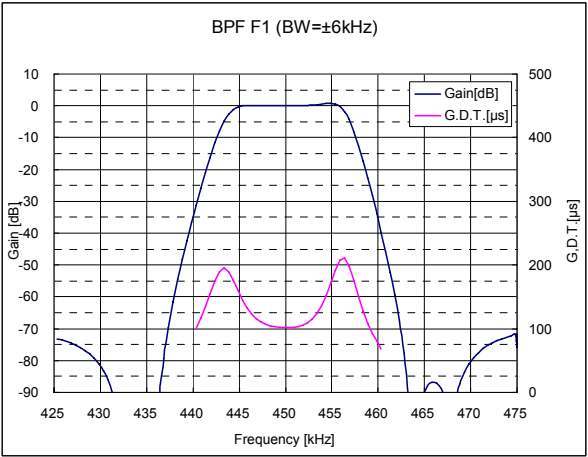
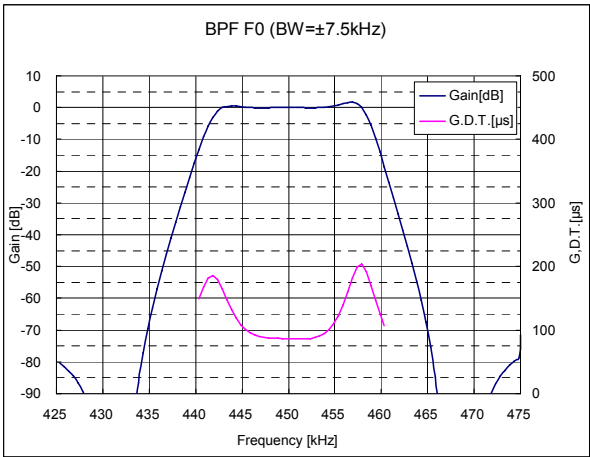
| Parameter                                                       | Condition       | Min. | Typ. | Max. | Units | Notes |
|-----------------------------------------------------------------|-----------------|------|------|------|-------|-------|
| Attenuation Characteristics<br>(relative to the gain at 450kHz) | 439kHz          |      |      | -50  | dB    |       |
|                                                                 | 445.5kHz        | -6   |      |      | dB    |       |
|                                                                 | 454.5kHz        | -6   |      |      | dB    |       |
|                                                                 | 461kHz          |      |      | -50  | dB    |       |
| Gain ripple                                                     | Within 450±3kHz |      |      | 3    | dB    |       |

## 7.4) F3 (H type)

| Parameter                                                       | Condition       | Min. | Typ. | Max. | Units | Notes |
|-----------------------------------------------------------------|-----------------|------|------|------|-------|-------|
| Attenuation Characteristics<br>(relative to the gain at 450kHz) | 441kHz          |      |      | -50  | dB    |       |
|                                                                 | 447kHz          | -6   |      |      | dB    |       |
|                                                                 | 453kHz          | -6   |      |      | dB    |       |
|                                                                 | 459kHz          |      |      | -50  | dB    |       |
| Gain ripple                                                     | Within 450±2kHz |      |      | 2    | dB    |       |

## 7.5) F4 (J type)

| Parameter                                                       | Condition         | Min. | Typ. | Max. | Units | Notes |
|-----------------------------------------------------------------|-------------------|------|------|------|-------|-------|
| Attenuation Characteristics<br>(relative to the gain at 450kHz) | 442.5kHz          |      |      | -50  | dB    |       |
|                                                                 | 448kHz            | -6   |      |      | dB    |       |
|                                                                 | 452kHz            | -6   |      |      | dB    |       |
|                                                                 | 457.5kHz          |      |      | -50  | dB    |       |
| Gain ripple                                                     | Within 450±1.5kHz |      |      | 2    | dB    |       |



8) IFBUF Characteristics

| Parameter     | Condition                                                                      | Min. | Typ. | Max. | Units | Notes |
|---------------|--------------------------------------------------------------------------------|------|------|------|-------|-------|
| Settling time | IFBUF to IFOUT,<br>IFBUF=0.32Vpp/step<br>C <sub>L2</sub> =21pF, {IFOG[1:0]}=00 |      | 100  |      | ns    |       |

Note: Convergence time within 1% when 0.32Vpp step signal input to IFBUF pin

## 14. Serial Interface Configuration

### 1) Register Configuration

| Name               | ADRS         | D7(MSB)    | D6      | D5          | D4          | D3            | D2 | D1          | D0(LSB) | W/R |
|--------------------|--------------|------------|---------|-------------|-------------|---------------|----|-------------|---------|-----|
| Control register 1 | 0x01         | BS[2:0]    |         |             | BAND        | BPF_BW[1:0]   |    | LOFREQ[1:0] |         | W/R |
|                    |              | 0          | 1       | 0           | 0           | 0             | 0  | 0           | 1       |     |
| Control register 2 | 0x02         | Reserved   |         |             |             | AGC_TIME[1:0] |    | AGC1_STEP   | CAL     | W/R |
|                    |              | 0          | 0       | 1           | 1           | 0             | 0  | 1           | 0       |     |
| Control register 3 | 0x03         | Reserved   |         |             |             |               |    | IFOG[1:0]   |         | W/R |
|                    |              | 0          | 0       | 0           | 0           | 0             | 0  | 0           | 0       |     |
| Software -reset    | 0x04         | SRST[7:0]  |         |             |             |               |    |             |         | W   |
|                    |              | —          | —       | —           | —           | —             | —  | —           | —       |     |
| Reserved           | 0x05 to 0x0A | Reserved   |         |             |             |               |    |             |         | —   |
| Control register 4 | 0x0B         | BPF_BW [2] | AGC_OFF | AGC1_G[5:0] |             |               |    |             |         | W/R |
|                    |              | 0          | 0       | 0           | 0           | 0             | 0  | 0           | 1       |     |
| Control register 5 | 0x0C         | Reserved   |         |             | AGC2_G[4:0] |               |    |             |         | W/R |
|                    |              | 1          | 0       | 0           | 0           | 0             | 0  | 0           | 0       |     |

Note: Do not access the data except specified address above.

## 2) Description of registers

## Address 0x01 (Control Register 1)

| Name               | D7(MSB) | D6 | D5 | D4   | D3          | D2 | D1          | D0(LSB) |
|--------------------|---------|----|----|------|-------------|----|-------------|---------|
| Control Register 1 | BS[2:0] |    |    | BAND | BPF_BW[1:0] |    | LOFREQ[1:0] |         |
| Initial Value      | 0       | 1  | 0  | 0    | 0           | 0  | 0           | 1       |

## BS[2:0]: Operation mode setting

| PDN pin | BS[2] | BS[1] | BS[0] | Mode name           | LDOD      | LDOA, AGNDIN | VREF      | MIX AGC, BPF, Divider | IFBUF     | Limiter, RSSI | DISCRI, Noise Squelch |
|---------|-------|-------|-------|---------------------|-----------|--------------|-----------|-----------------------|-----------|---------------|-----------------------|
| 0       | -     | -     | -     | Mode 0 (Power-down) | OFF       | OFF          | OFF       | OFF                   | OFF       | OFF           | OFF                   |
| 1       | 0     | 0     | 1     | Mode 1 (Standby 1)  | <u>ON</u> | OFF          | OFF       | OFF                   | OFF       | OFF           | OFF                   |
| 1       | 0     | 1     | 0     | Mode 2 (Standby 2)  | <u>ON</u> | <u>ON</u>    | OFF       | OFF                   | OFF       | OFF           | OFF                   |
| 1       | 0     | 1     | 1     | Mode 3              | <u>ON</u> | <u>ON</u>    | <u>ON</u> | OFF                   | OFF       | OFF           | OFF                   |
| 1       | 1     | 0     | 0     | Mode 4              | <u>ON</u> | <u>ON</u>    | <u>ON</u> | <u>ON</u>             | <u>ON</u> | OFF           | OFF                   |
| 1       | 1     | 0     | 1     | Mode 5              | <u>ON</u> | <u>ON</u>    | <u>ON</u> | <u>ON</u>             | <u>ON</u> | <u>ON</u>     | OFF                   |
| 1       | 1     | 1     | 0     | Mode 6              | <u>ON</u> | <u>ON</u>    | <u>ON</u> | <u>ON</u>             | OFF       | <u>ON</u>     | <u>ON</u>             |
| 1       | 1     | 1     | 1     | Mode 7              | <u>ON</u> | <u>ON</u>    | <u>ON</u> | <u>ON</u>             | <u>ON</u> | <u>ON</u>     | <u>ON</u>             |

Note: Do not set the combination of the code which is not defined in the table given above.

## BAND: Demodulated signal level setting

| BAND | Function |
|------|----------|
| 0    | Narrow   |
| 1    | Wide     |

Note1: When {BAND} register is set to "0", demodulated signal level at AUDIOOUT pin, when input signal is  $\Delta f = \pm 1.5\text{kHz}$  dev, is 100mVrms typ. When {BAND} register is set to "1", demodulated signal level at AUDIOOUT pin, when input signal is  $\Delta f = \pm 3.0\text{kHz}$  dev, is 100mVrms typ.

## BPF\_BW[1:0]: BPF band width setting

| BPF_BW [2] | BPF_BW [1] | BPF_BW [0] | name | 6dB attenuation     | Attenuation band width |
|------------|------------|------------|------|---------------------|------------------------|
| 1          | 0/1        | 0/1        | F0   | $\pm 7.5\text{kHz}$ | $\pm 15\text{kHz}$     |
| 0          | 0          | 0          | F1   | $\pm 6\text{kHz}$   | $\pm 12.5\text{kHz}$   |
| 0          | 0          | 1          | F2   | $\pm 4.5\text{kHz}$ | $\pm 11\text{kHz}$     |
| 0          | 1          | 0          | F3   | $\pm 3\text{kHz}$   | $\pm 9\text{kHz}$      |
| 0          | 1          | 1          | F4   | $\pm 2\text{kHz}$   | $\pm 7.5\text{kHz}$    |

## LOFREQ[1:0]: Local frequency setting

| LOFREQ<br>[1] | LOFREQ<br>[0] | Local frequency |
|---------------|---------------|-----------------|
| 0             | 0             | 45.9MHz         |
| 0             | 1             | 50.4MHz         |
| 1             | 0             | 57.6MHz         |

Note: Do not set the combination of the code which is not defined in the table given above.

## Address 0x02 (Control Register 2)

| Name               | D7(MSB)  | D6 | D5 | D4 | D3            | D2 | D1        | D0(LSB) |
|--------------------|----------|----|----|----|---------------|----|-----------|---------|
| Control Register 2 | Reserved |    |    |    | AGC_TIME[1:0] |    | AGC1_STEP | CAL     |
| Initial Value      | 0        | 0  | 1  | 1  | 0             | 0  | 1         | 0       |

## AGC\_TIME[1:0]: AGC response time setting

This register sets response time for AGC1 gain and AGC2 gain to change by 1 step.

| AGC_TIME<br>[1] | AGC_TIME<br>[0] | AGC response time [ms] |         |         |                     |         |         |
|-----------------|-----------------|------------------------|---------|---------|---------------------|---------|---------|
|                 |                 | AGC1_STEP=0 setting    |         |         | AGC1_STEP=1 setting |         |         |
|                 |                 | State A                | State B | State C | State A             | State B | State C |
| 0               | 0               | 0.56                   | 8.50    | 8.50    | 0.38                | 4.35    | 4.35    |
| 0               | 1               | 0.92                   | 8.79    | 8.79    | 0.56                | 4.50    | 4.50    |
| 1               | 0               | 1.64                   | 9.37    | 9.37    | 0.93                | 4.79    | 4.79    |
| 1               | 1               | 3.08                   | 10.52   | 10.52   | 1.66                | 5.38    | 5.38    |

Note 1: Values above indicate response time during AGC gain changes from maximum to minimum or from minimum to maximum.

State A: AGC1 output level is beyond the upper limit.

State B: AGC1 output level is within the upper limit and AGC2 output level is beyond the upper limit.

State C: AGC2 output level is under the lower limit.

| Data      | Function                                                | Operation |       | Notes |
|-----------|---------------------------------------------------------|-----------|-------|-------|
|           |                                                         | 0         | 1     |       |
| AGC1_STEP | AGC1 gain switching range setting                       | ±1dB      | ±2dB  |       |
| CAL       | Discriminator circuit calibration start trigger (Note2) | Invalid   | Start |       |

Note 2: calibration is performed synchronized with the rising edge of {CAL}. After calibration is completed, this register is set to "0" automatically. It takes 1.3ms before calibration is completed. Refer to "calibration procedure" for further information.

## Address 0x03 (Control Register 3)

| Name               | D7(MSB)  | D6 | D5 | D4 | D3 | D2 | D1        | D0(LSB) |
|--------------------|----------|----|----|----|----|----|-----------|---------|
| Control Register 3 | Reserved |    |    |    |    |    | IFOG[1:0] |         |
| Initial Value      | 0        | 0  | 0  | 0  | 0  | 0  | 0         | 0       |

## IFOG[1:0]: IFBUF Gain setting

| IFOG [1] | IFOG [0] | IFBUF Gain[dB] |
|----------|----------|----------------|
| 0        | 0        | 6              |
| 0        | 1        | 9              |
| 1        | 0        | 12             |
| 1        | 1        | 15             |

## Address 0x04 (Software Reset)

| Name           | D7(MSB)   | D6 | D5 | D4 | D3 | D2 | D1 | D0(LSB) |
|----------------|-----------|----|----|----|----|----|----|---------|
| Software-reset | SRST[7:0] |    |    |    |    |    |    |         |
| Initial Value  | —         | —  | —  | —  | —  | —  | —  | —       |

When data 0x04:10101010 is written to the SRST[7:0] register, software reset is performed.  
Refer to System Reset for further information.

## Address 0x0B (Control Register 4)

| Name               | D7(MSB)    | D6      | D5          | D4 | D3 | D2 | D1 | D0(LSB) |
|--------------------|------------|---------|-------------|----|----|----|----|---------|
| Control Register 4 | BPF_BW [2] | AGC_OFF | AGC1_G[5:0] |    |    |    |    |         |
| Initial Value      | 0          | 0       | 0           | 0  | 0  | 0  | 0  | 1       |

| Data        | Function             | Operation                       |                                  | Notes                         |
|-------------|----------------------|---------------------------------|----------------------------------|-------------------------------|
|             |                      | 0                               | 1                                |                               |
| BPF_BW[2]   | F0<br>(±7.5kHz)      | OFF                             | ON                               |                               |
| AGC_OFF     | AGC function         | Disable<br>(AGC Auto operation) | Enable<br>(AGC manual operation) |                               |
| AGC1_G[5:0] | AGC1 gain adjustment | 21 to -19dB by 1dB step         |                                  | Available only<br>{AGC_OFF}=1 |

| AGC1_G[5] | AGC1_G[4] | AGC1_G[3] | AGC1_G[2] | AGC1_G[1] | AGC1_G[0] | Gain [dB] |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0         | 1         | 0         | 1         | 0         | 1         | 21        |
| 0         | 1         | 0         | 1         | 0         | 0         | 20        |
| 0         | 1         | 0         | 0         | 1         | 1         | 19        |
| 0         | 1         | 0         | 0         | 1         | 0         | 18        |
| 0         | 1         | 0         | 0         | 0         | 1         | 17        |
| 0         | 1         | 0         | 0         | 0         | 0         | 16        |
| 0         | 0         | 1         | 1         | 1         | 1         | 15        |
| 0         | 0         | 1         | 1         | 1         | 0         | 14        |
| 0         | 0         | 1         | 1         | 0         | 1         | 13        |
| 0         | 0         | 1         | 1         | 0         | 0         | 12        |
| 0         | 0         | 1         | 0         | 1         | 1         | 11        |
| 0         | 0         | 1         | 0         | 1         | 0         | 10        |
| 0         | 0         | 1         | 0         | 0         | 1         | 9         |
| 0         | 0         | 1         | 0         | 0         | 0         | 8         |
| 0         | 0         | 0         | 1         | 1         | 1         | 7         |
| 0         | 0         | 0         | 1         | 1         | 0         | 6         |
| 0         | 0         | 0         | 1         | 0         | 1         | 5         |
| 0         | 0         | 0         | 1         | 0         | 0         | 4         |
| 0         | 0         | 0         | 0         | 1         | 1         | 3         |
| 0         | 0         | 0         | 0         | 1         | 0         | 2         |
| 0         | 0         | 0         | 0         | 0         | 1         | 1         |
| 0         | 0         | 0         | 0         | 0         | 0         | 0         |
| 1         | 1         | 1         | 1         | 1         | 1         | -1        |
| 1         | 1         | 1         | 1         | 1         | 0         | -2        |
| 1         | 1         | 1         | 1         | 0         | 1         | -3        |
| 1         | 1         | 1         | 1         | 0         | 0         | -4        |
| 1         | 1         | 1         | 0         | 1         | 1         | -5        |
| 1         | 1         | 1         | 0         | 1         | 0         | -6        |
| 1         | 1         | 1         | 0         | 0         | 1         | -7        |
| 1         | 1         | 1         | 0         | 0         | 0         | -8        |
| 1         | 1         | 0         | 1         | 1         | 1         | -9        |
| 1         | 1         | 0         | 1         | 1         | 0         | -10       |
| 1         | 1         | 0         | 1         | 0         | 1         | -11       |
| 1         | 1         | 0         | 1         | 0         | 0         | -12       |
| 1         | 1         | 0         | 0         | 1         | 1         | -13       |
| 1         | 1         | 0         | 0         | 1         | 0         | -14       |
| 1         | 1         | 0         | 0         | 0         | 1         | -15       |
| 1         | 1         | 0         | 0         | 0         | 0         | -16       |
| 1         | 0         | 1         | 1         | 1         | 1         | -17       |
| 1         | 0         | 1         | 1         | 1         | 0         | -18       |
| 1         | 0         | 1         | 1         | 0         | 1         | -19       |

Note: Do not set the combination of the code which is not defined in the table given above.

## Address 0x0C (Control Register 5)

| Name               | D7(MSB)  | D6 | D5 | D4          | D3 | D2 | D1 | D0(LSB) |
|--------------------|----------|----|----|-------------|----|----|----|---------|
| Control Register 5 | Reserved |    |    | AGC2_G[4:0] |    |    |    |         |
| Initial Value      | 1        | 0  | 0  | 0           | 0  | 0  | 0  | 0       |

| Data        | Function             | Operation             |   | Notes                         |
|-------------|----------------------|-----------------------|---|-------------------------------|
|             |                      | 0                     | 1 |                               |
| AGC2_G[4:0] | AGC2 gain adjustment | 12 to 0dB by 1dB step |   | Available only<br>{AGC_OFF}=1 |

| AGC2_G[4] | AGC2_G[3] | AGC2_G[2] | AGC2_G[1] | AGC2_G[0] | Gain [dB] |
|-----------|-----------|-----------|-----------|-----------|-----------|
| 0         | 1         | 1         | 0         | 0         | 12        |
| 0         | 1         | 0         | 1         | 1         | 11        |
| 0         | 1         | 0         | 1         | 0         | 10        |
| 0         | 1         | 0         | 0         | 1         | 9         |
| 0         | 1         | 0         | 0         | 0         | 8         |
| 0         | 0         | 1         | 1         | 1         | 7         |
| 0         | 0         | 1         | 1         | 0         | 6         |
| 0         | 0         | 1         | 0         | 1         | 5         |
| 0         | 0         | 1         | 0         | 0         | 4         |
| 0         | 0         | 0         | 1         | 1         | 3         |
| 0         | 0         | 0         | 1         | 0         | 2         |
| 0         | 0         | 0         | 0         | 1         | 1         |
| 0         | 0         | 0         | 0         | 0         | 0         |

Note: Do not set the combination of the code which is not defined in the table given above.

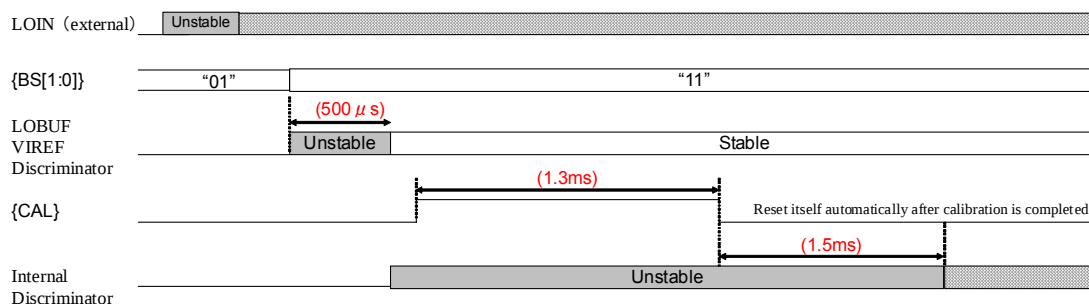
## 15. Calibration Procedure

AK2365 employs a function to calibrate free-running frequency of VCO in Discriminator and demodulated signal level. Before starting RX Operation, calibration is required in order to acquire proper VCO operation range and demodulated signal level.

Following procedure is required before calibration.

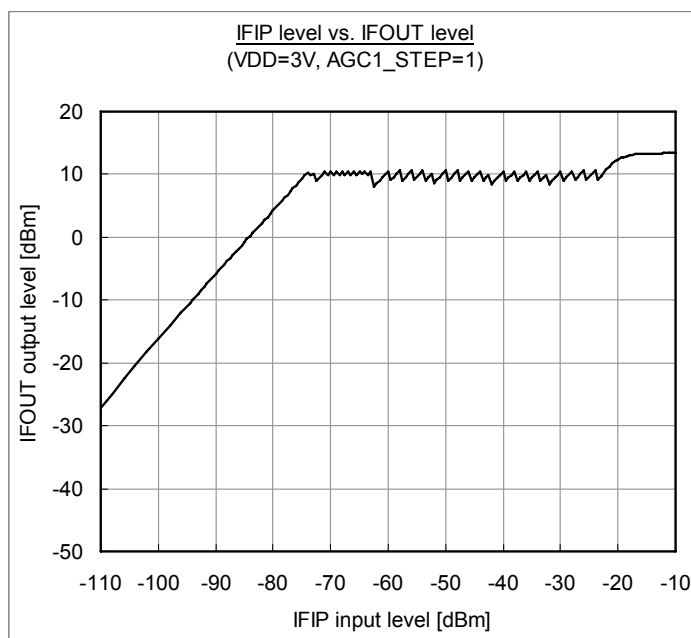
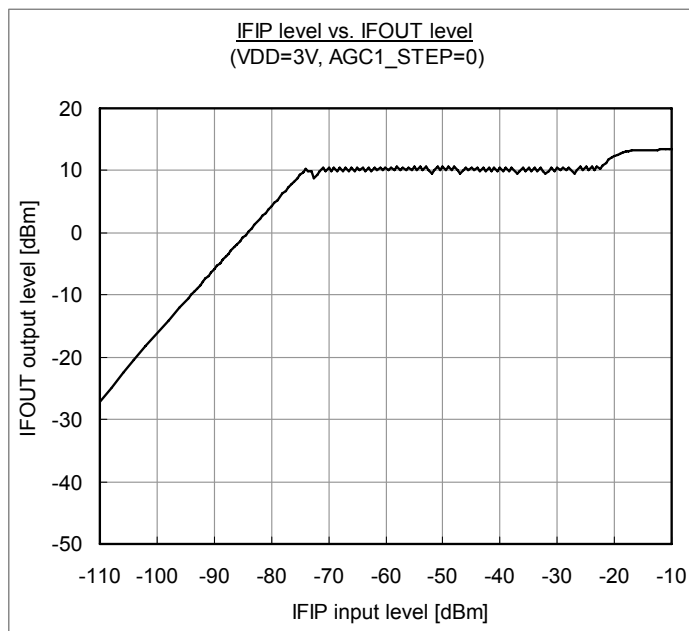
- <1> Start up the external TCXO and continuously supply LO signal to AK2365.
- <2> Set "110" to 0x01 {BS[2:0]} and start up all circuits. After this operation, the circuits necessary for calibration (LOBUF, VIREF, Discriminator) will be powered on and calibration can be possible in 500us.
- <3> Calibration is begun by setting "1" to address 0x02 {CAL}. When the calibration is executed once, the calibration operation cannot be stopped excluding master reset. Even if "0" is written in {CAL}, the calibration is completely executed.
- <4> Calibration data is maintained excluding the time when the master reset is executed or DVDD power supply is down.
- <5> It takes 1.5ms for Discriminator to become steady after the calibration is completed.

### Power-up sequence recommendation



## 16. AGC Operation

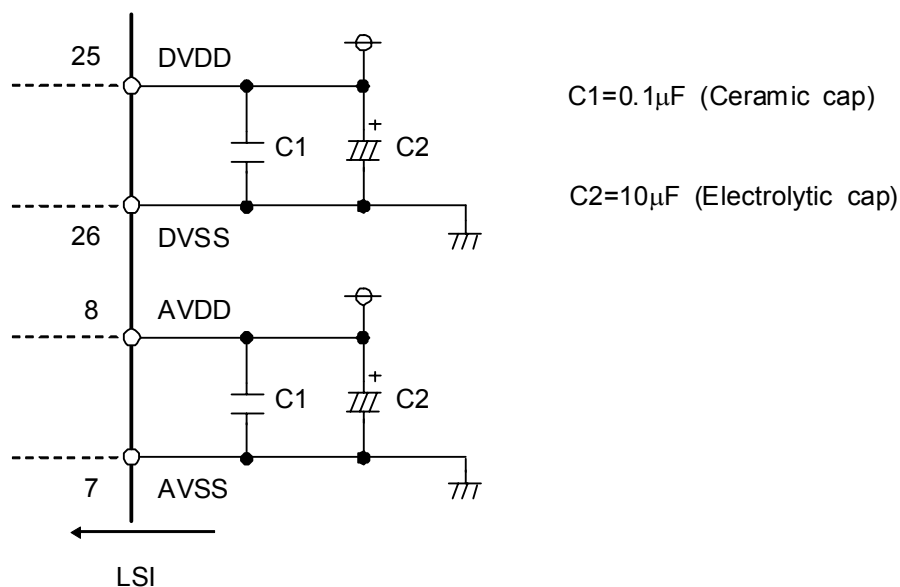
AK2365 has two AGC circuits, AGC1 and AGC2. The signal level from IFIP pin is adjustable automatically by AGC1/2. The following graphs show IFIP input vs. IFOUT output characteristics by setting {AGC1\_STEP}=0/1, {IFOG[1:0]}=00, {AGC\_OFF}=0. Setting {AGC\_OFF}=1 can disable automatic gain adjustable operation and also enable manual gain operation by {AGC1\_G[5:0]}, {AGC2\_G[4:0]} registers.



## 17. Recommended External Application Circuits

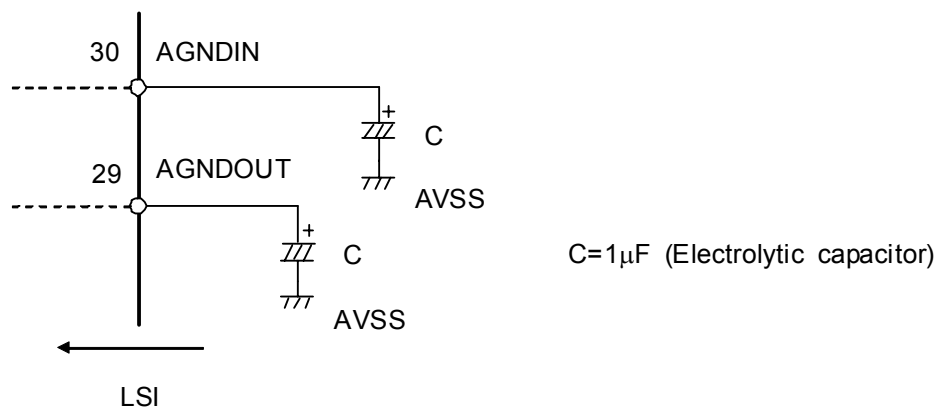
### 1) Power supply stabilizing capacitors

Connect capacitors between VDD and VSS pins to eliminate ripple and noise included in power supply. For maximum effect, the capacitors should be placed at a shortest distance between the pins.

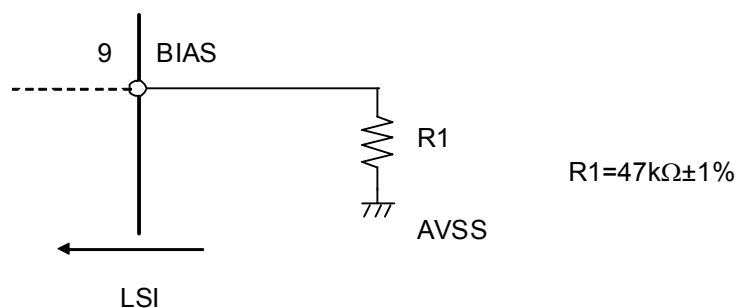


### 2) AGND stabilizing capacitors

It is recommended that capacitors with 1 $\mu$ F or larger be connected between VSS and the AGND and AGNDIN pins to stabilize the AGND signal. The capacitors must be placed as close to the pins as possible.

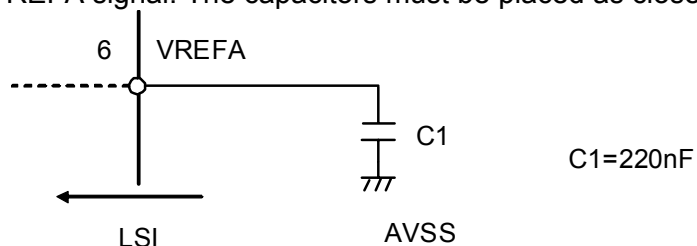


### 3) BIAS pin



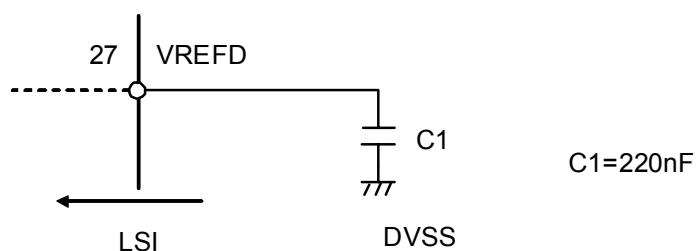
## 4) VREFA output

It is recommended that capacitors with 220nF or larger be connected between AVSS and VREFA pin to stabilize the VREFA signal. The capacitors must be placed as close to the pins as possible.

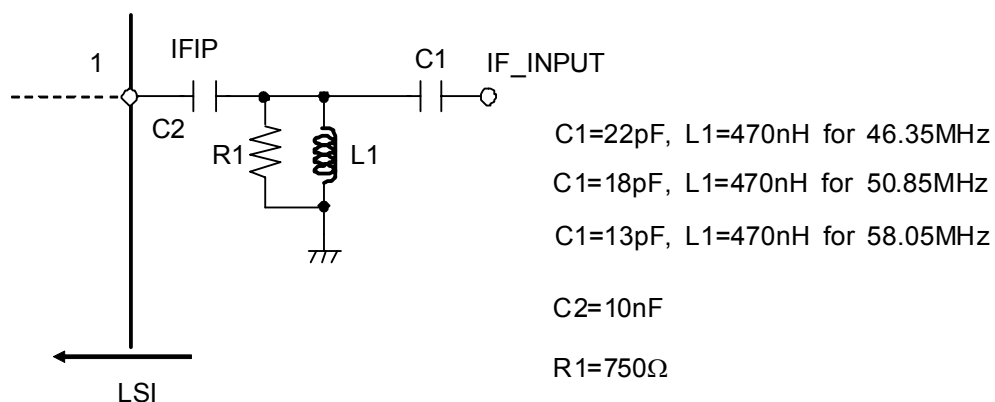


## 5) VREFD output

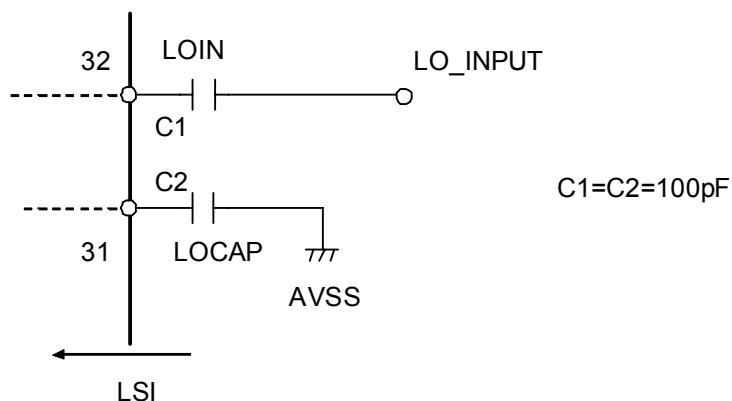
It is recommended that capacitors with 220nF or larger be connected between DVSS and VREFD pin to stabilize the VREFD signal. The capacitors must be placed as close to the pins as possible.



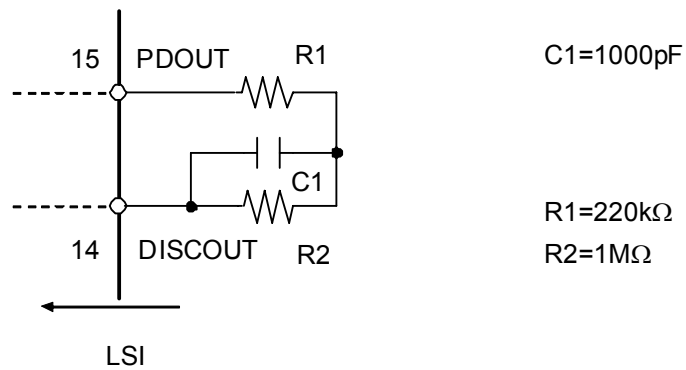
## 6) MIX



## 7) LOIN

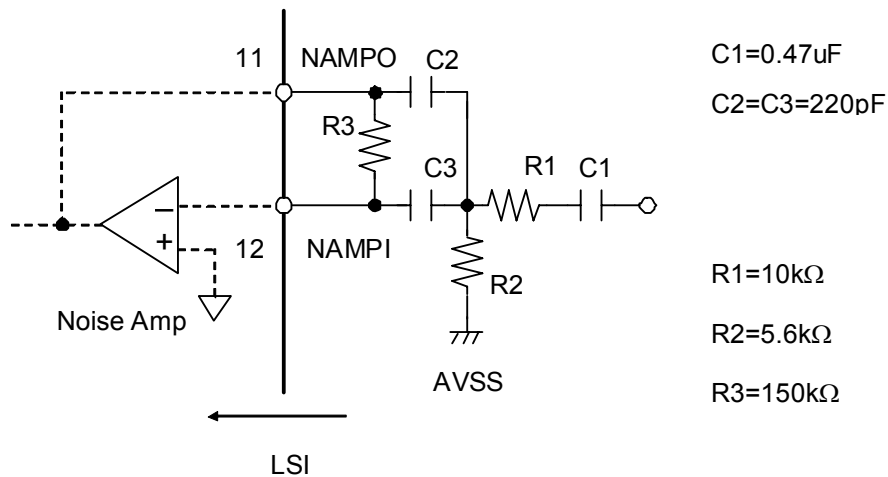


## 8) Discriminator



## 9) Noise AMP

The following gives a sample configuration of a BPF when input frequency is 31kHz. Some parameters can be calculated using following (1) to (3) equations.



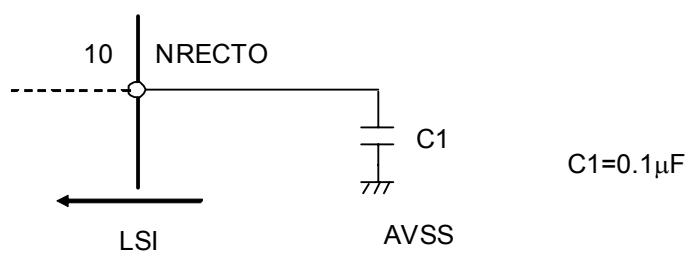
$$(1) \quad f_0 = \frac{1}{2\pi\sqrt{R_3(R_1 // R_2)C^2}}$$

$$(2) \quad G_v = \frac{R_3}{2R_1}$$

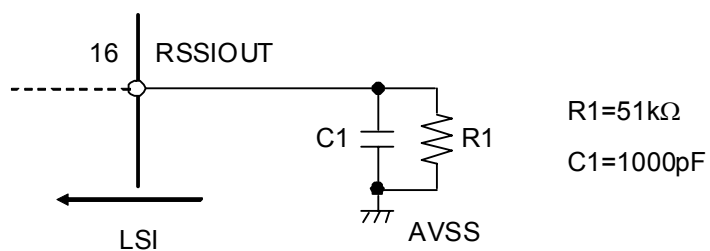
$$(3) \quad Q^2 = \frac{R_3}{4(R_1 // R_2)}$$

## 10) NECTO pin

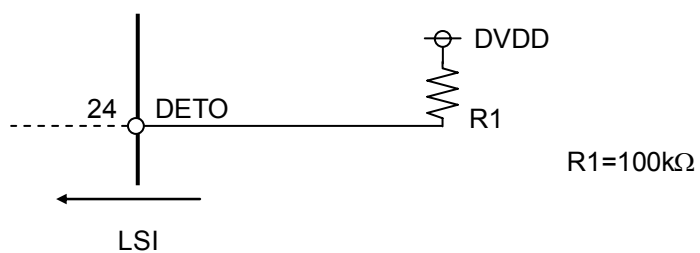
Rise time of noise detection is proportionate to  $C1=0.1\mu\text{F}$  and internal resistance  $75\text{k}\Omega$



## 11) RSSIOUT pin

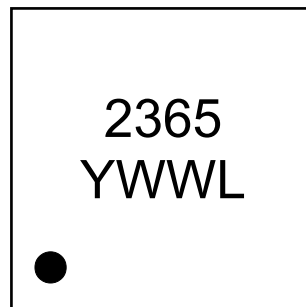


## 12) DETO



## 18. Packaging

### ☐ Marking



[Contents of YWWL]

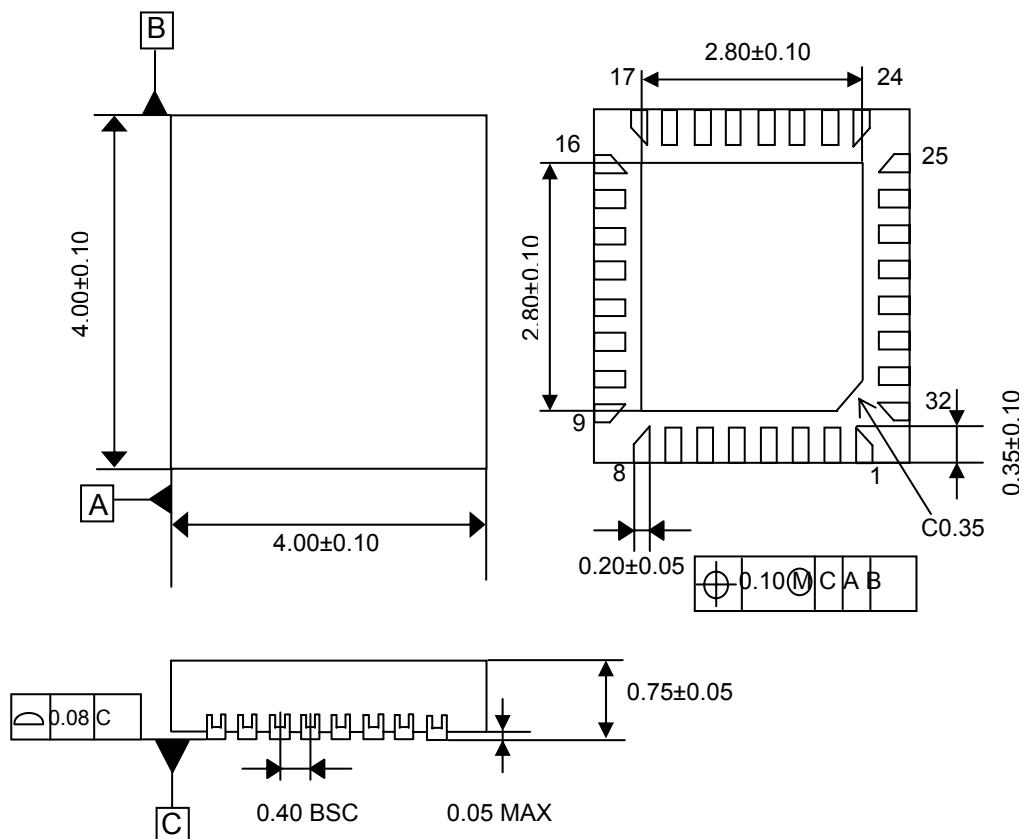
Y: Last digit of calendar year. (Year 2011->1, 2012->2)

WW: Manufacturing week number.

L: Lot identification, given to each product lot which is made in a week.  
LOT ID is given in alphabetical order (A, B, C...).

### ☐ Mechanical Outline

Package : 32pin QFN (4.0 x 4.0 x 0.7mm, 0.4mm pitch)



Note) The exposure pad(Exposed Pad) of the center of the package back is connected to opening or VSS.

## 19. Important Notice

### IMPORTANT NOTICE

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