

# DATA SHEET

## **74ABT16260**

12-bit to 24-bit multiplexed D-type latch  
(3-State)

Product data

2002 Apr 03

Replaces 74ABT16260/74ABTH16260 dated 1998 Feb 10

## 12-bit to 24-bit multiplexed D-type latch (3-State)

## 74ABT16260

## FEATURES

- ESD protection exceeds 2000 V per Mil-Std-883C, Method 3015; exceeds 200 V using machine model (C = 200 pF, R = 0).
- Latch-up performance exceeds 500 mA per JEDEC Standard JESD-17.
- Distributed  $V_{CC}$  and GND pin configuration minimizes high-speed switching noise.
- Flow-through architecture optimizes PCB layout.
- High-drive outputs (–32 mA  $I_{OH}$ , 64 mA  $I_{OL}$ ).
- Package options:
  - 56-pin plastic Shrink Small-Outline Package (SSOP)
  - 56-pin plastic Thin Shrink Small-Outline Package (TSSOP)

## DESCRIPTION

The 74ABT16260 is a 12-bit to 24-bit multiplexed D-type latch used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. This device is also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output enable ( $\overline{OE1B}$ ,  $\overline{OE2B}$ , and  $\overline{OE A}$ ) inputs control the bus transceiver functions. The  $\overline{OE1B}$  and  $\overline{OE2B}$  control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch enable input is HIGH, the latch is transparent. When the latch enable input goes LOW, the data present at the inputs is latched and remains latched until the latch enable input is returned HIGH.

To ensure the high-impedance state during power-up or power-down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

## QUICK REFERENCE DATA

| SYMBOL                 | PARAMETER                                     | CONDITIONS<br>$T_{amb} = 25^{\circ}\text{C}$ ; GND = 0V | TYPICAL    | UNIT          |
|------------------------|-----------------------------------------------|---------------------------------------------------------|------------|---------------|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>nAx to nBx    nBx to nAx | $C_L = 50 \text{ pF}$                                   | 2.8<br>2.5 | ns            |
| $C_{IN}$               | Input capacitance                             | $V_I = 0 \text{ V or } V_{CC}$                          | 4          | pF            |
| $C_{OUT}$              | Output capacitance                            | $V_{IO} = 0 \text{ V or } 5.0 \text{ V}$                | 6          | pF            |
| $I_{CCZ}$              | Total supply current                          | Outputs disabled                                        | 100        | $\mu\text{A}$ |

## ORDERING INFORMATION

| PACKAGES                     | TEMPERATURE RANGE | ORDER CODE    | DWG NUMBER |
|------------------------------|-------------------|---------------|------------|
| 56-Pin Plastic SSOP Type III | –40 °C to +85 °C  | 74ABT16260DL  | SOT371-1   |
| 56-Pin Plastic TSSOP Type II | –40 °C to +85 °C  | 74ABT16260DGG | SOT364-1   |

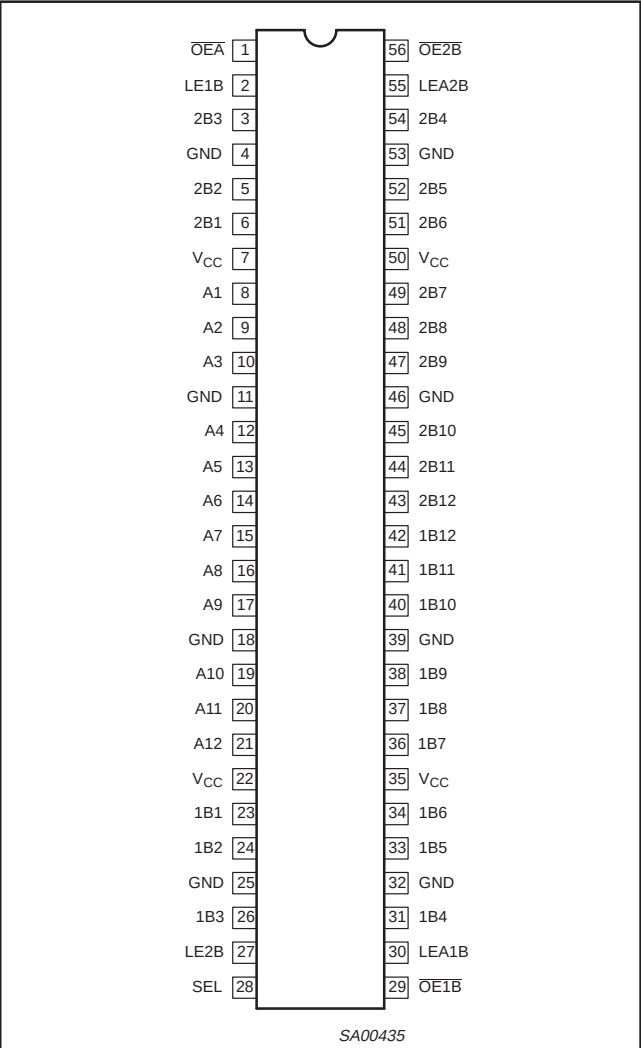
## PIN DESCRIPTION

| PIN NUMBER                                     | SYMBOL                                                    | FUNCTION                         |
|------------------------------------------------|-----------------------------------------------------------|----------------------------------|
| 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21   | A <sub>n</sub>                                            | Data inputs/outputs (A)          |
| 23, 24, 26, 31, 33, 34, 36, 37, 38, 40, 41, 42 | 1B <sub>n</sub>                                           | Data inputs/outputs (B1)         |
| 6, 5, 3, 54, 52, 51, 49, 48, 47, 45, 44, 43    | 2B <sub>n</sub>                                           | Data inputs/outputs (B2)         |
| 1, 29, 56                                      | $\overline{OE A}$ , $\overline{OE1B}$ , $\overline{OE2B}$ | Output enable input (Active-LOW) |
| 2, 27, 30, 55                                  | LE1B, LE2B, LEA1B, LEA2B                                  | Latch enable inputs              |

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PIN CONFIGURATION



FUNCTION TABLES

B to A ( $\overline{OE\overline{B}} = H$ )

| INPUTS |    |     |      |      |                             | OUTPUT |
|--------|----|-----|------|------|-----------------------------|--------|
| 1B     | 2B | SEL | LE1B | LE2B | $\overline{OE\overline{A}}$ | A      |
| H      | X  | H   | H    | X    | L                           | H      |
| L      | X  | H   | H    | X    | L                           | L      |
| X      | X  | H   | L    | X    | L                           | A0     |
| X      | H  | L   | X    | H    | L                           | H      |
| X      | L  | L   | X    | H    | L                           | L      |
| X      | X  | L   | X    | L    | L                           | A0     |
| X      | X  | X   | X    | X    | H                           | Z      |

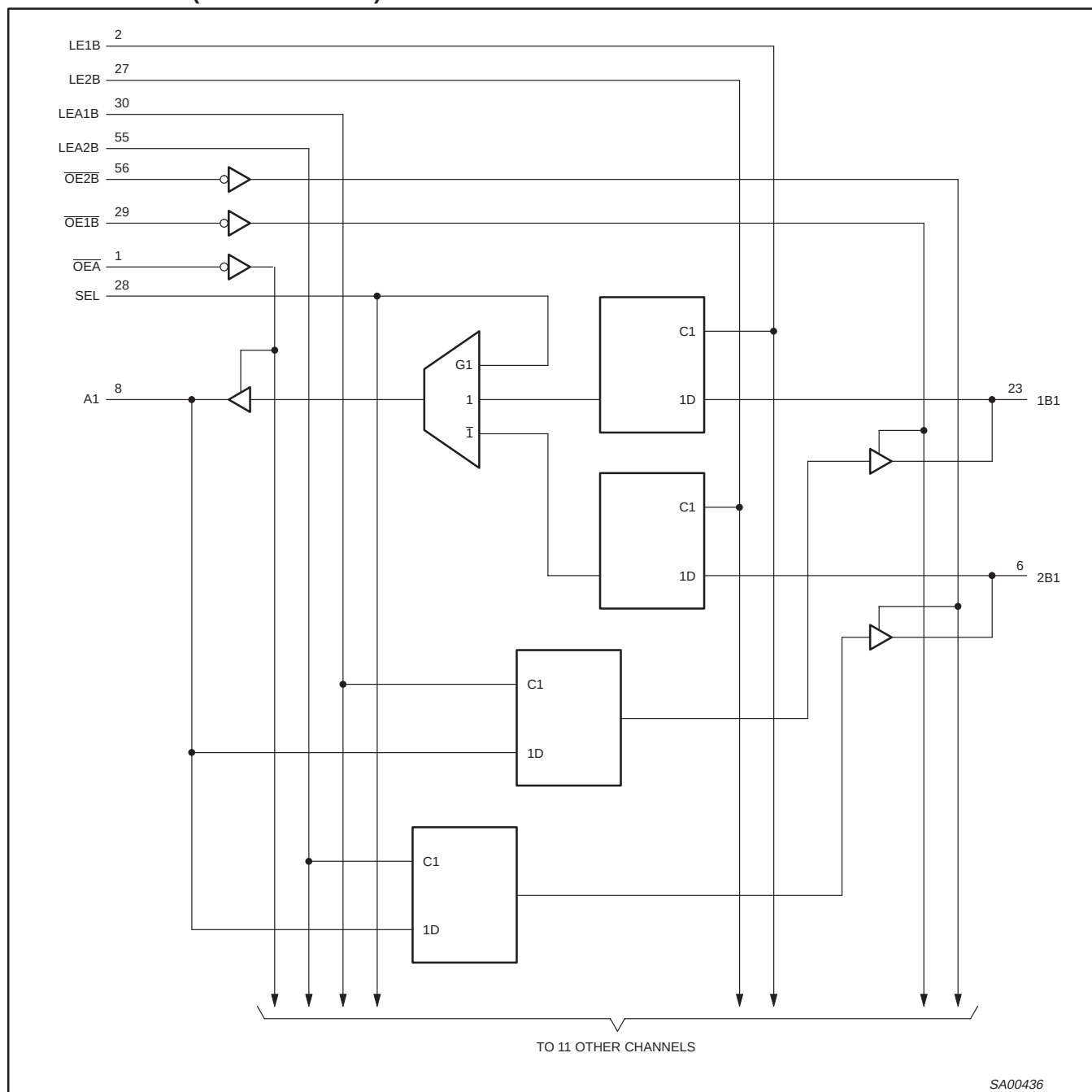
A to B ( $\overline{OE\overline{A}} = H$ )

| INPUTS |       |       |                              |                              | OUTPUT |        |
|--------|-------|-------|------------------------------|------------------------------|--------|--------|
| A      | LEA1B | LEA2B | $\overline{OE1\overline{B}}$ | $\overline{OE2\overline{B}}$ | 1B     | 2B     |
| H      | H     | H     | L                            | L                            | H      | H      |
| L      | H     | H     | L                            | L                            | L      | L      |
| H      | H     | L     | L                            | L                            | H      | 2B0    |
| L      | H     | L     | L                            | L                            | L      | 2B0    |
| H      | L     | H     | L                            | L                            | 1B0    | H      |
| L      | L     | H     | L                            | L                            | 1B0    | L      |
| X      | L     | L     | L                            | L                            | 1B0    | 2B0    |
| X      | X     | X     | H                            | H                            | Z      | Z      |
| X      | X     | X     | L                            | H                            | Active | Z      |
| X      | X     | X     | H                            | L                            | Z      | Active |
| X      | X     | X     | L                            | L                            | Active | Active |

## 12-bit to 24-bit multiplexed D-type latch (3-State)

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## LOGIC DIAGRAM (POSITIVE LOGIC)



## 12-bit to 24-bit multiplexed D-type latch (3-State)

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**ABSOLUTE MAXIMUM RATINGS**Over operating free-air temperature range (unless otherwise specified)<sup>1</sup>

| SYMBOL           | PARAMETER                                                                | CONDITIONS         | LIMITS |      | UNIT |
|------------------|--------------------------------------------------------------------------|--------------------|--------|------|------|
|                  |                                                                          |                    | MIN    | MAX  |      |
| V <sub>CC</sub>  | Supply voltage range                                                     |                    | −0.5   | 7    | V    |
| V <sub>I</sub>   | Input voltage range                                                      | see Note 2         | −0.5   | 7    | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the HIGH state or power-off state |                    | −0.5   | 5.5  | V    |
| I <sub>O</sub>   | Current into any output in the LOW state                                 |                    | −      | 128  | mA   |
| I <sub>IK</sub>  | Input clamp current                                                      | V <sub>I</sub> < 0 | −      | −18  | mA   |
| I <sub>OK</sub>  | Output clamp current                                                     | V <sub>O</sub> < 0 | −      | −50  | mA   |
|                  | Maximum power dissipation at T <sub>amb</sub> = 55 °C (in still air)     | see Note 3         | −      | 1.4  | W    |
| T <sub>stg</sub> | Storage temperature range                                                |                    | −65    | +150 | °C   |

**NOTES:**

- Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The maximum package power dissipation is calculated using a junction temperature of 150 °C and a board trace length of 750 mils.

**RECOMMENDED OPERATING CONDITIONS<sup>1</sup>**

| SYMBOL              | PARAMETER                          |                 | LIMITS |                 | UNIT |
|---------------------|------------------------------------|-----------------|--------|-----------------|------|
|                     |                                    |                 | MIN    | MAX             |      |
| V <sub>CC</sub>     | Supply voltage                     |                 | 4.5    | 5.5             | V    |
| V <sub>IH</sub>     | HIGH-level input voltage           |                 | 2      | −               | V    |
| V <sub>IL</sub>     | LOW-level input voltage            |                 | −      | 0.8             | V    |
| V <sub>I</sub>      | Input voltage                      |                 | 0      | V <sub>CC</sub> | V    |
| I <sub>OH</sub>     | HIGH-level output current          |                 | −      | −32             | mA   |
| I <sub>OL</sub>     | LOW-level output current           |                 | −      | 64              | mA   |
| ΔtΔ/v               | Input transition rise or fall rate | Outputs enabled | −      | 10              | ns/V |
| ΔtΔ/V <sub>CC</sub> | Power-up ramp rate                 |                 | 200    | −               | μs/V |
| T <sub>amb</sub>    | Operating free-air temperature     |                 | −40    | +85             | °C   |

**NOTE:**

- Unused or floating inputs must be held HIGH or LOW.

## 12-bit to 24-bit multiplexed D-type latch (3-State)

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## DC ELECTRICAL CHARACTERISTICS

| SYMBOL                           | PARAMETER                                            | TEST CONDITIONS                                                                                                              |              | LIMITS                    |       |      |                                        |      | UNIT |
|----------------------------------|------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------|--------------|---------------------------|-------|------|----------------------------------------|------|------|
|                                  |                                                      |                                                                                                                              |              | T <sub>amb</sub> = +25 °C |       |      | T <sub>amb</sub> = −40 °C<br>to +85 °C |      |      |
|                                  |                                                      |                                                                                                                              |              | Min                       | Typ   | Max  | Min                                    | Max  |      |
| V <sub>IK</sub>                  | Input clamp voltage                                  | V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = −18 mA                                                                            |              | –                         | −0.8  | −1.2 | –                                      | −1.2 | V    |
| V <sub>OH</sub>                  | HIGH-level output voltage                            | V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = −3 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                        |              | 2.5                       | 2.9   | –    | 2.5                                    | –    | V    |
|                                  |                                                      | V <sub>CC</sub> = 5.0 V; I <sub>OH</sub> = −3 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                        |              | 3.0                       | 3.4   | –    | 3.0                                    | –    | V    |
|                                  |                                                      | V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = −32 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                       |              | 2.0                       | 2.4   | –    | 2.0                                    | –    | V    |
| V <sub>OL</sub>                  | LOW-level output voltage                             | V <sub>CC</sub> = 4.5 V; I <sub>OL</sub> = 64 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                        |              | –                         | 0.42  | 0.55 | –                                      | 0.55 | V    |
| I <sub>I</sub>                   | Input leakage current                                | V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND                                                             | Control pins | –                         | ±0.01 | ±1   | –                                      | ±1   | μA   |
|                                  |                                                      | V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND                                                             | Data pins    | –                         |       | ±3   | –                                      | ±5   | μA   |
| I <sub>OFF</sub>                 | Power-off leakage current                            | V <sub>CC</sub> = 0.0 V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5 V                                                            |              | –                         | ±5.0  | ±100 | –                                      | ±100 | μA   |
| I <sub>PU</sub> /I <sub>PD</sub> | Power-up/down 3-State output current                 | V <sub>CC</sub> = 2.0 V; V <sub>O</sub> = 0.5 V; V <sub>I</sub> = GND or V <sub>CC</sub> ; V <sub>OE</sub> = V <sub>CC</sub> |              | –                         | ±60   | ±200 | –                                      | ±200 | μA   |
| I <sub>OZH</sub>                 | 3-State output HIGH current                          | V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 2.7 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                         |              | –                         | 1.0   | 10   | –                                      | 10   | μA   |
| I <sub>OZL</sub>                 | 3-State output LOW current                           | V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 0.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                         |              | –                         | −1.0  | −10  | –                                      | −10  | μA   |
| I <sub>CEX</sub>                 | Output HIGH leakage current                          | V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>                                     |              | –                         |       | 50   | –                                      | 50   | μA   |
| I <sub>O</sub>                   | Output current <sup>1</sup>                          | V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 2.5 V                                                                              |              | −50                       | −100  | −225 | −50                                    | −225 | mA   |
| I <sub>CC</sub>                  | Quiescent supply current                             | V <sub>CC</sub> = 5.5 V; Outputs HIGH, V <sub>I</sub> = GND or V <sub>CC</sub>                                               |              | –                         | 0.2   | 1.5  | –                                      | 1.5  | mA   |
|                                  |                                                      | V <sub>CC</sub> = 5.5 V; Outputs LOW, V <sub>I</sub> = GND or V <sub>CC</sub>                                                |              | –                         | 8     | 19   | –                                      | 19   | mA   |
|                                  |                                                      | V <sub>CC</sub> = 5.5 V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>                                            |              | –                         | 0.1   | 1.0  | –                                      | 1.0  | mA   |
| ΔI <sub>CC</sub>                 | Additional supply current per input pin <sup>2</sup> | Outputs enabled, one input at 3.4 V, other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V                         |              | –                         | 0.1   | 1.5  | –                                      | 1.5  | mA   |

## NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

## 12-bit to 24-bit multiplexed D-type latch (3-State)

74ABT16260

**AC ELECTRICAL CHARACTERISTICS**

Over recommended operating free-air temperature range (unless otherwise noted).

| SYMBOL    | PARAMETER       |             | $V_{CC} = 5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ |     |     | $T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$ |     | UNIT |
|-----------|-----------------|-------------|-------------------------------------------------------------|-----|-----|-------------------------------------------------------------------------|-----|------|
|           | FROM (INPUT)    | TO (OUTPUT) | MIN                                                         | TYP | MAX | MIN                                                                     | MAX |      |
| $t_{PLH}$ | A or B          | B or A      | 1                                                           | 2.8 | 4.8 | 1                                                                       | 5.6 | ns   |
| $t_{PHL}$ |                 |             | 1                                                           | 2.5 | 5   | 1                                                                       | 5.9 | ns   |
| $t_{PLH}$ | $\overline{LE}$ | A or B      | 1.1                                                         | 3.2 | 4.9 | 1.1                                                                     | 5.8 | ns   |
| $t_{PHL}$ |                 |             | 1.1                                                         | 3.2 | 4.9 | 1.1                                                                     | 5.3 | ns   |
| $t_{PLH}$ | SEL (B1)        | A           | 1.3                                                         | 3.2 | 4.6 | 1.3                                                                     | 5.3 | ns   |
|           | SEL (B2)        | A           | 1.1                                                         | 2.8 | 4.9 | 1.1                                                                     | 6   | ns   |
| $t_{PHL}$ | SEL (B1)        | A           | 1.5                                                         | 3.0 | 4.4 | 1.5                                                                     | 4.4 | ns   |
|           | SEL (B2)        | A           | 1.6                                                         | 2.6 | 5.1 | 1.6                                                                     | 5.9 | ns   |
| $t_{PZH}$ | $\overline{OE}$ | A or B      | 1                                                           | 2.9 | 4.7 | 1                                                                       | 5.7 | ns   |
| $t_{PZL}$ |                 |             | 1.6                                                         | 2.2 | 5.1 | 1.6                                                                     | 5.8 | ns   |
| $t_{PHZ}$ | $\overline{OE}$ | A or B      | 2.2                                                         | 4.1 | 5.4 | 2.2                                                                     | 6.4 | ns   |
| $t_{PLZ}$ |                 |             | 1.3                                                         | 3.2 | 4.4 | 1.3                                                                     | 4.8 | ns   |

**AC SETUP CHARACTERISTICS**

Over recommended operating free-air temperature range (unless otherwise noted).

| SYMBOL   | PARAMETER                                             | $V_{CC} = 5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ |     | $T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$ |     | UNIT |
|----------|-------------------------------------------------------|-------------------------------------------------------------|-----|-------------------------------------------------------------------------|-----|------|
|          |                                                       | MIN                                                         | MAX | MIN                                                                     | MAX |      |
| $t_w$    | Pulse duration, LE1B, LE2B, LEA1B, or LEA2B HIGH      | 3.3                                                         | —   | 3.3                                                                     | —   | ns   |
| $t_{su}$ | Set-up time, data before LE1B, LE2B, LEA1B, or LEA2B↓ | 1.5                                                         | —   | 1.5                                                                     | —   | ns   |
| $t_h$    | Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓    | 1                                                           | —   | 1                                                                       | —   | ns   |

12-bit to 24-bit multiplexed D-type latch (3-State)

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AC WAVEFORMS

$V_M = 1.5\text{ V}$  for all waveforms  
The outputs are measured one at a time with one transition per measurement.

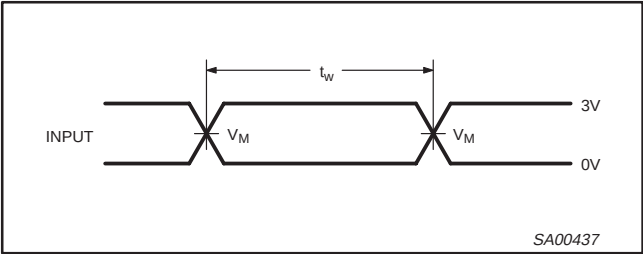


Figure 1. Pulse duration

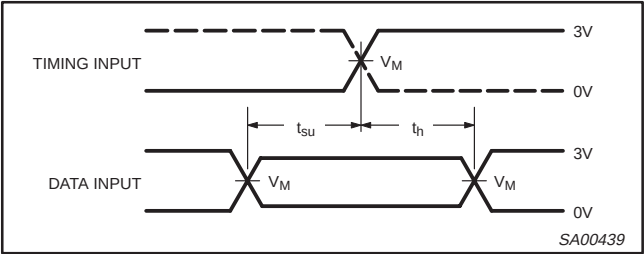
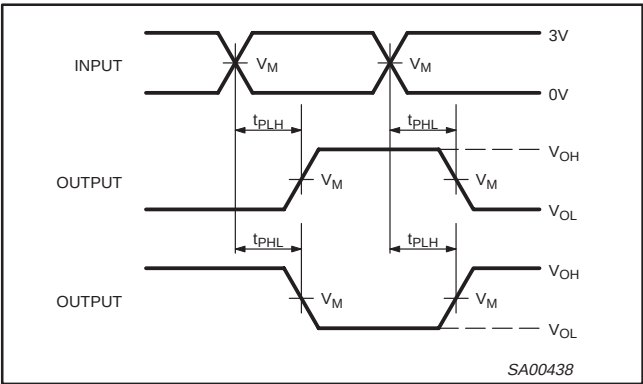
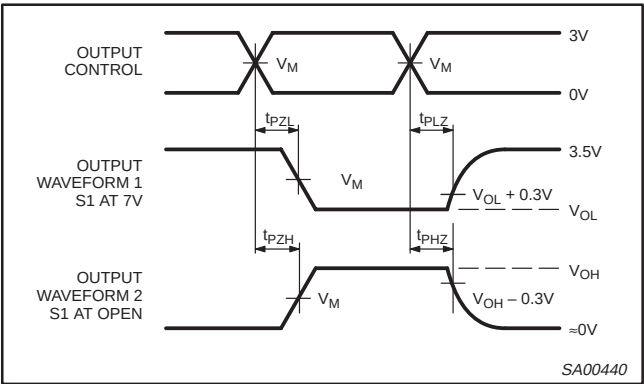


Figure 3. Set-up and hold times



All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .

Figure 2. Propagation delay times; inverting and non-inverting outputs



Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Figure 4. Enable and disable times; LOW- and HIGH-level enabling

TEST LOAD CIRCUIT

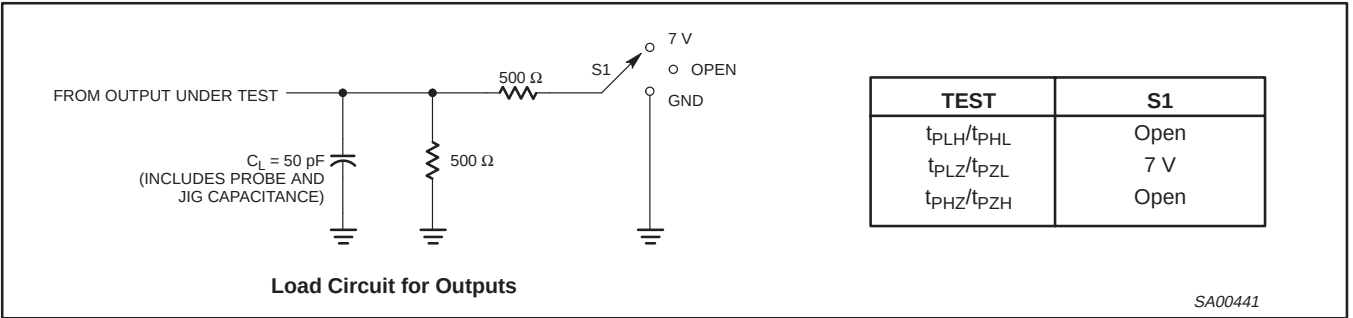


Figure 5. Test load circuit

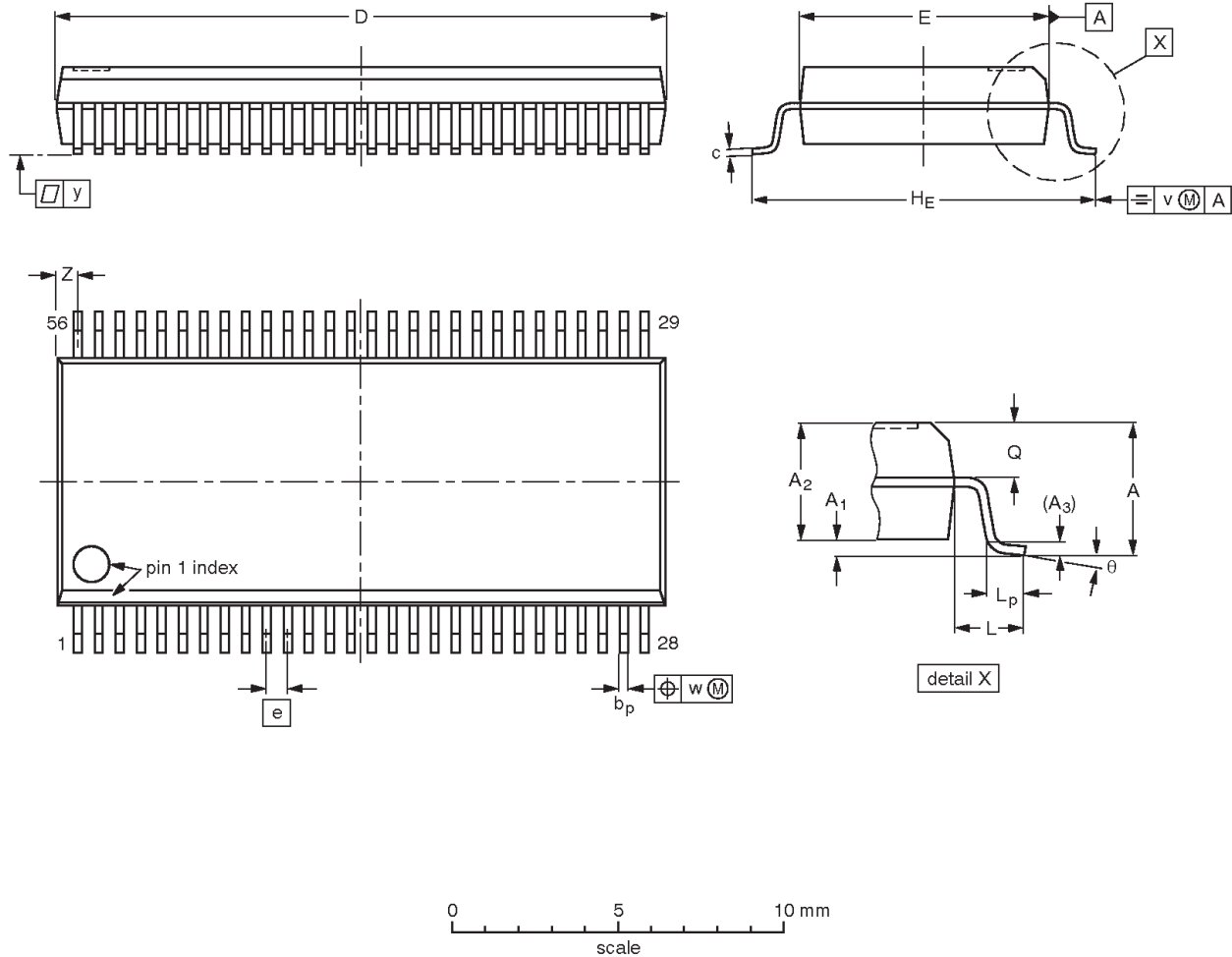


12-bit to 24-bit multiplexed D-type latch (3-State)

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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A<br>max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L   | L <sub>p</sub> | Q          | v    | w    | y   | Z <sup>(1)</sup> | θ        |
|------|-----------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-------|----------------|-----|----------------|------------|------|------|-----|------------------|----------|
| mm   | 2.8       | 0.4<br>0.2     | 2.35<br>2.20   | 0.25           | 0.3<br>0.2     | 0.22<br>0.13 | 18.55<br>18.30   | 7.6<br>7.4       | 0.635 | 10.4<br>10.1   | 1.4 | 1.0<br>0.6     | 1.2<br>1.0 | 0.25 | 0.18 | 0.1 | 0.85<br>0.40     | 8°<br>0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

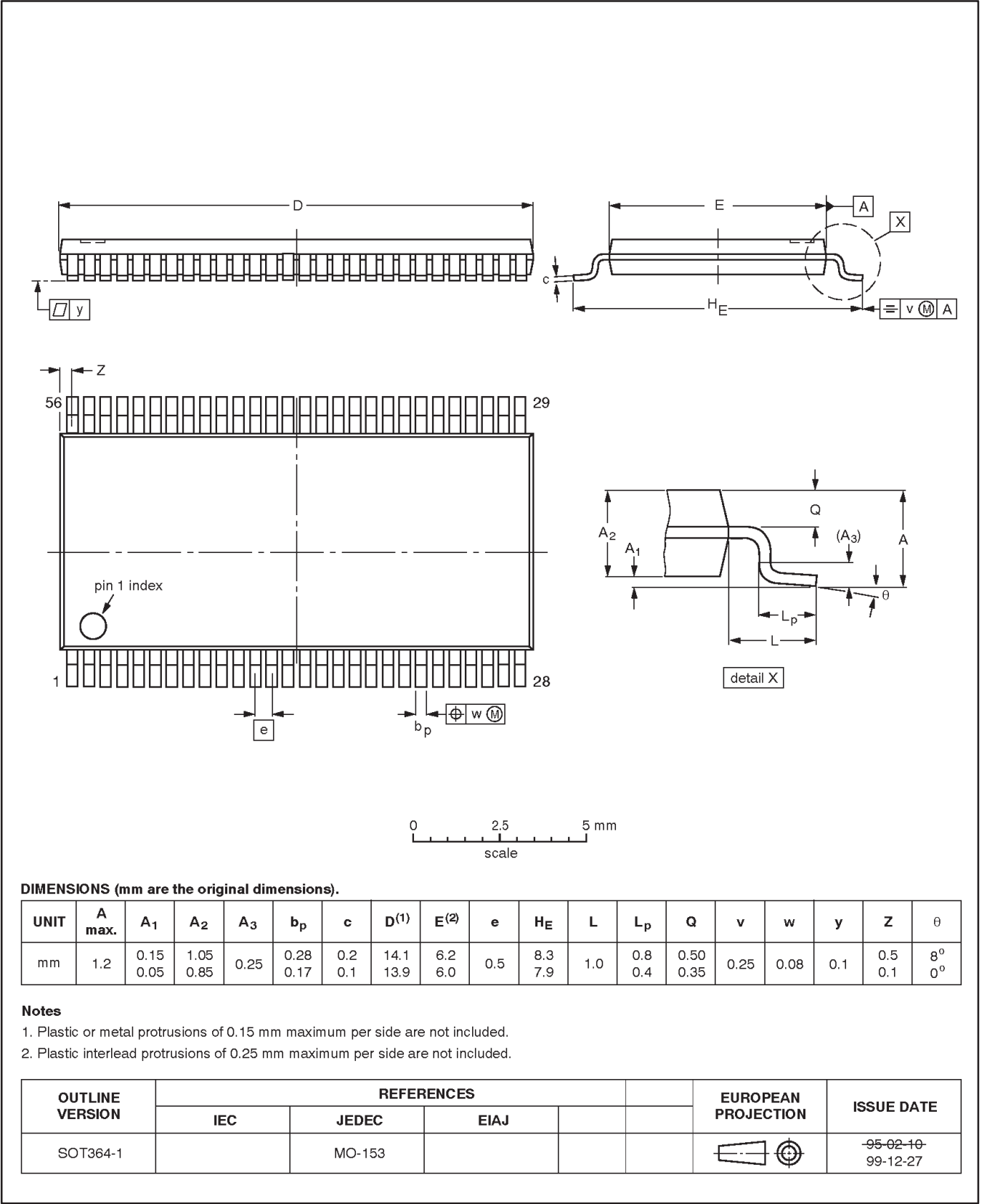
| OUTLINE<br>VERSION | REFERENCES |        |      |  | EUROPEAN<br>PROJECTION                                                                | ISSUE DATE           |
|--------------------|------------|--------|------|--|---------------------------------------------------------------------------------------|----------------------|
|                    | IEC        | JEDEC  | EIAJ |  |                                                                                       |                      |
| SOT371-1           |            | MO-118 |      |  |  | 95-02-04<br>99-12-27 |

12-bit to 24-bit multiplexed D-type latch (3-State)

74ABT16260

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



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12-bit to 24-bit multiplexed D-type latch (3-State)

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**NOTES**

## 12-bit to 24-bit multiplexed D-type latch (3-State)

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## Data sheet status

| Data sheet status <sup>[1]</sup> | Product status <sup>[2]</sup> | Definitions                                                                                                                                                                                                                                                                                                            |
|----------------------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Objective data                   | Development                   | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.                                                                                                                            |
| Preliminary data                 | Qualification                 | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.                                     |
| Product data                     | Production                    | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A. |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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