EMC1462

3.3V Multiple Channel 1°C Digital Temperature Sensor with Beta Compensation

Features

- Programmable SMBus Address
- Support for Diodes Requiring the BJT Transistor model:
  - Supports 45 nm, 65 nm and 90 nm CPU Thermal Diodes
- Pin Compatible with EMC1412 and EMC1442
- Automatically Determines External Diode Type and Optimal Settings
- Resistance Error Correction
- Up to One External Temperature Monitor
  - ±1°C Maximum Accuracy ($20°C<T_{DIODE}<110°C$)
  - 0.125°C Resolution
- Supports up to 2.2 nF Diode Filter Capacitor
- Internal Temperature Monitor
  - ±1°C Accuracy
  - 0.125°C Resolution
- 3.3V Supply Voltage
- Programmable Temperature Limits for:
  - $\overline{\text{ALERT}}$: +85°C Default High Limit and 0°C Default Low Limit
  - $\overline{\text{THERM}}$: +125°C Default
- Available in the Following Package Types:
  - 8-Lead 2 mm x 3 mm TDFN
  - 8-Lead 2 mm x 2mm WDFN
- Lead-free RoHS Compliant Package

Applications

- Notebook Computers
- Desktop Computers
- Industrial
- Embedded Applications

Description

The EMC1462 is a high-accuracy, low-cost, System Management Bus (SMBus) temperature sensor. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT Transistor model including 45 nm, 65 nm and 90 nm processors) and automatic diode type detection combine to provide a robust solution for complex environmental monitoring applications.

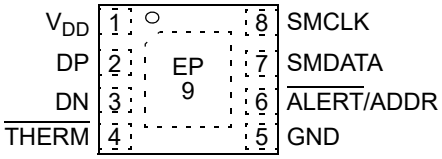
The EMC1462 monitors two temperature channels (one external and one internal), providing ±1°C accuracy for both external and internal diode temperatures.

REC automatically eliminates the temperature error caused by series resistance, allowing greater flexibility in routing thermal diodes. Beta Compensation eliminates temperature errors caused by low, variable beta transistors common in today's geometry processors. The automatic beta detection feature monitors the external diode/transistor and determines the optimum sensor settings for accurate temperature measurements, regardless of processor technology. This frees the user from providing unique sensor configurations for each temperature monitoring application.

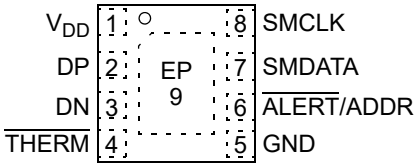
These advanced features, plus ±1°C measurement accuracy, provide a low-cost, highly flexible and accurate solution for critical temperature monitoring applications.

Package Type

EMC1462
8-Lead TDFN*

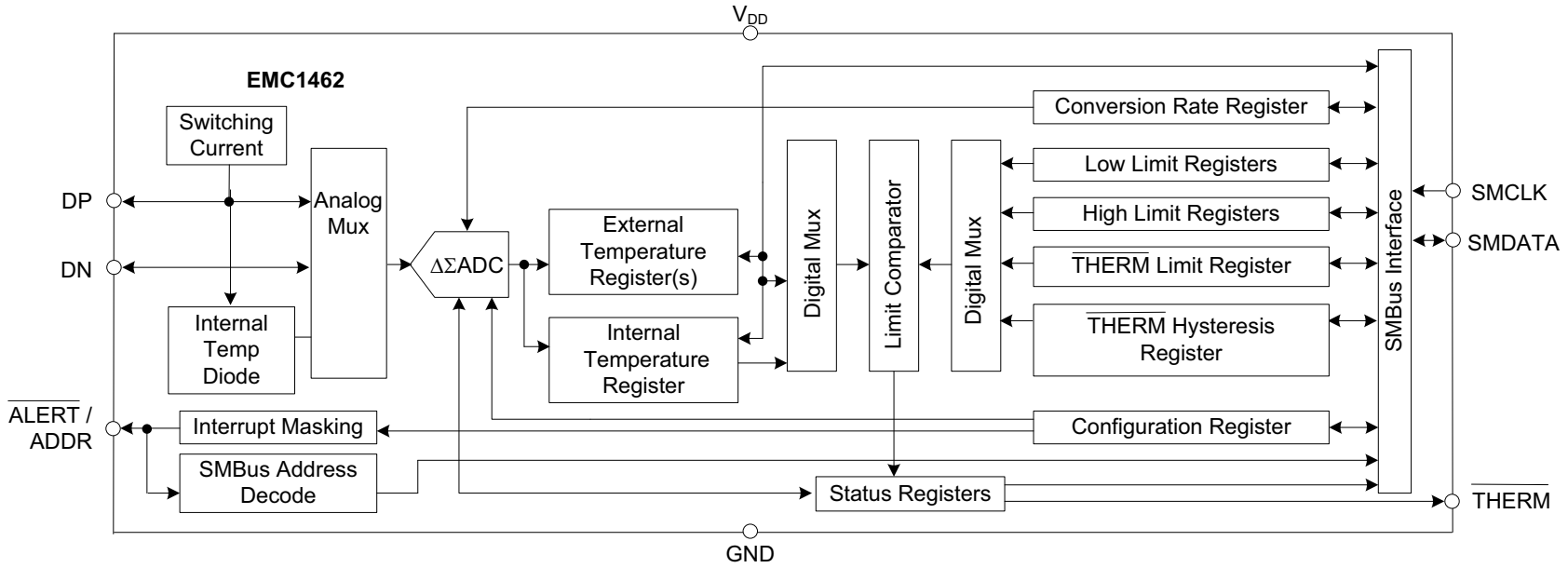


EMC1462
8-Lead WDFN*



* Includes Exposed Thermal Pad (EP); see Table 3-1

EMC1462 – Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

Supply Voltage (V_{DD}) ..... -0.3V to +4.0V
Voltage on 5V Tolerant Pins (V_{5VT_pin}) ..... -0.3V to +5.5V
Voltage on 5V Tolerant Pins ($|V_{5VT\_pin}-V_{DD}|$) **(Note 1)** ..... 0V to +3.6V
Voltage on Any Other Pin to Ground ..... -0.3V to V_{DD}+0.3V
Operating Temperature ..... -40°C to +125°C
Storage Temperature ..... -55°C to +150°C
Junction Temperature (T_J) ..... +150°C
ESD Protection on All Pins (HBM) ..... ±2000V
Thermal Resistance ..... 89°C/W

Note 1: For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, THERM and ALERT), the pull-up voltage must not exceed 3.6V when the device is unpowered.

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all limits apply for typical values at ambient temperature 1.65V ≤ V_{DD} ≤ +2.75V at -40°C ≤ T_A ≤ +125°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	—
Supply Current	I_{DD}	—	430	850	µA	One conversion/second, dynamic averaging disabled
		—	930	1200	µA	Four conversions/second, dynamic averaging disabled
		—	1120	—	µA	≥16 conversions/second, dynamic averaging enabled
Standby Supply Current	I_{DD}	—	170	230	µA	Device in Standby mode, no active SMBus communications, ALERT and THERM pins not asserted.
Internal Temperature Monitor						
Temperature Accuracy	—	—	±0.25	±1	°C	-5°C < T_A < +100°C
		—	—	±2	°C	-40°C < T_A < +125°C
Temperature Resolution	—	—	±0.125	—	°C	—
External Temperature Monitor						
Temperature Accuracy	—	—	±0.25	±1	°C	+20°C < T_{DIODE} < +110°C, 0°C < T_A < +100°C
		—	—	±2	°C	-40°C < T_{DIODE} < +127°C
Temperature Resolution	—	—	±0.125	—	°C	—
Conversion Time, All Channels	t_{CONV}	—	190	—	ms	Default settings
Capacitive Filter	C_{FILTER}	—	2.2	2.7	nF	Connected across external diode

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits apply for typical values at ambient temperature 1.65V ≤ V_{DD} ≤ +2.75V at -40°C ≤ T_A ≤ +125°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
$\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ Pins						
Output Low Voltage	V_{OL}	0.4	—	—	V	I_{SINK} = 8 mA
Leakage Current	I_{LEAK}	—	—	±5	µA	$\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins, Device powered or unpowered, T_A < +85°C, pull-up voltage ≤ 2.75V

SMBUS ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, GND = Ground, V_{DD}=3.0V, T_A=-40°C TO 125°C, all typical values are at T_A=27°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
SMBus Interface						
Input High Voltage	V_{IH}	2.0	—	V_{DD}	V	5V Tolerant
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	5V Tolerant
Leakage Current	I_{LEAK}	—	—	±5	µA	Powered or unpowered T_A < 85°C
Hysteresis	—	—	420	—	mV	—
Input Capacitance	C_{IN}	—	5	—	pF	—
Output Low Sink Current	I_{OL}	8.2	—	15	mA	SMDATA = 0.4V
SMBus Timing						
Clock Frequency	f_{SMB}	10	—	400	kHz	—
Spike Suppression	t_{SP}	—	—	50	ns	—
Bus Free Time Stop to Start	t_{BUF}	1.3	—	—	µs	—
Hold Time: Start	$t_{HD:STA}$	0.6	—	—	µs	—
Setup Time: Start	$t_{SU:STA}$	0.6	—	—	µs	—
Setup Time: Stop	$t_{SU:STO}$	0.6	—	—	µs	—
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	µs	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	—
Clock Low Period	t_{LOW}	1.3	—	—	µs	—
Clock High Period	t_{HIGH}	0.6	—	—	µs	—
Clock/Data Fall Time	t_{FALL}	—	—	300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise Time	t_{RISE}	—	—	300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}	—	—	400	pF	Per BUS line
Timeout	$t_{TIMEOUT}$	25	—	35	ms	Disabled by default

TEMPERATURE CHARACTERISTICS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	—
Storage Temperature Range	T_A	-55	—	+150	°C	—
Thermal Package Resistances						
Thermal Resistance, TDFN 8LD 2 mm x 3 mm	θ_{JA}	—	89	—	°C/W	—
Thermal Resistance, WDFN 8LD 2 mm x 2 mm	θ_{JA}	—	89	—	°C/W	—

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and, therefore, outside the warranted range.

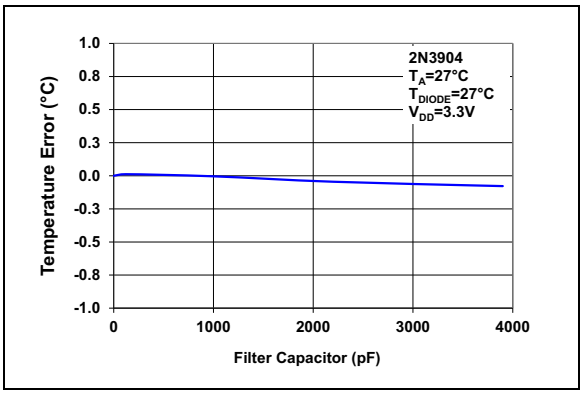


FIGURE 2-1: *Temperature Error vs. Filter Capacitor.*

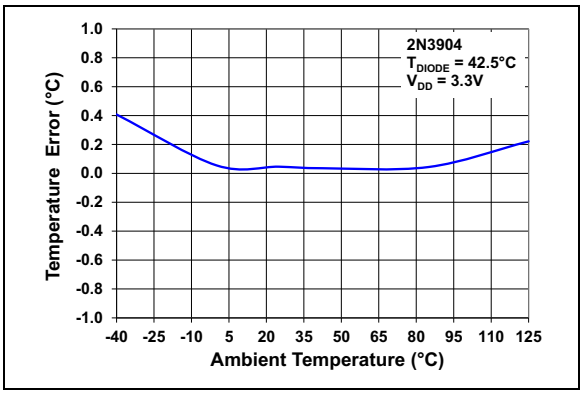


FIGURE 2-4: *Temperature Error vs. Ambient Temperature.*

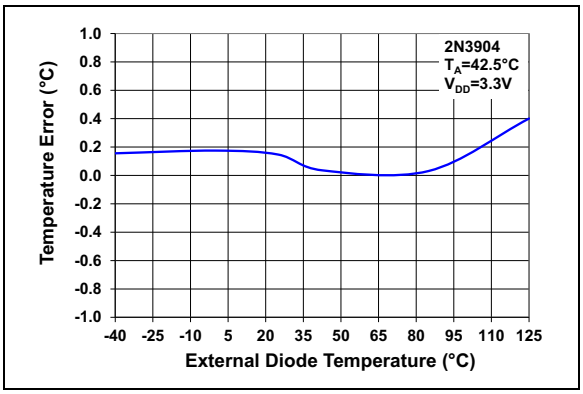


FIGURE 2-2: *Temperature Error vs. External Diode Temperature.*

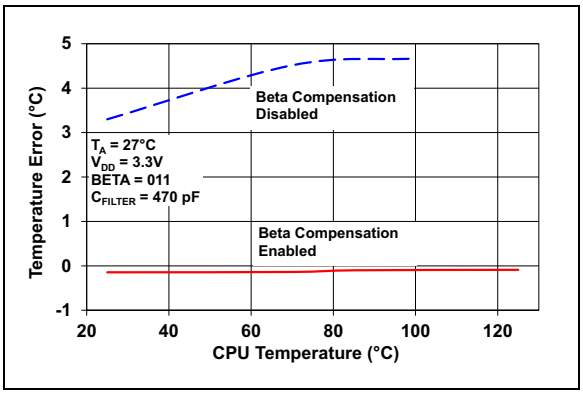


FIGURE 2-5: *Temperature Error vs. CPU Temperature.*

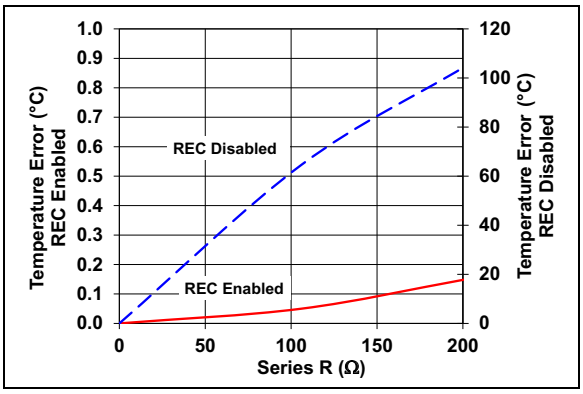


FIGURE 2-3: *Temperature Error vs. Series Resistance.*

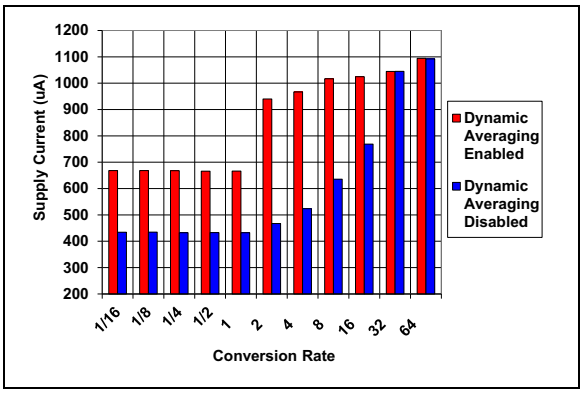


FIGURE 2-6: *Supply Current vs. Conversion Rate.*

NOTES:

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Symbol	Type	Description
1	V_{DD}	P	Power Pin
2	DP	AIO	External diode positive (anode) connection
3	DN	AIO	External diode negative (cathode) connection
4	$\overline{\text{THERM}}$[1]	OD (5V)	Active low critical $\overline{\text{THERM}}$ output signal. Requires pull-up resistor
5	GND	P	Ground
6	$\overline{\text{ALERT}}$/ADDR	OD (5V)	$\overline{\text{ALERT}}$[1] - Active low digital $\overline{\text{ALERT}}$ output signal. Requires pull-up resistor.
			ADDR - Selects SMBus address, based on pull-up resistor.
7	SMDATA[1]	DIOD (5V)	SMBus Data input/output. Requires pull-up resistor.
8	SMCLK[1]	DI (5V)	SMBus Clock input. Requires pull-up resistor.
9	EP	P	Exposed Thermal Pad. Not internally connected, but grounding is recommended.

Note 1: For the 5V tolerant pins that have a pull-up resistor ($\overline{\text{ALERT}}$, $\overline{\text{THERM}}$, SMCLK and SMDATA), the voltage difference between V_{DD} and the pull-up voltage must never exceed 3.6V.

The pin types are described in Table 3-2.

TABLE 3-2: PIN TYPES

Pin Type	Description
P	This pin is used to supply power or ground to the device.
AIO	Analog Input/Output. This pin is used as an I/O for analog signals.
DI	Digital Input. This pin is used as a digital input. This pin is 5V tolerant.
DIOD	Digital Input/Open Drain Output. This pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output. This pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

NOTES:

4.0 FUNCTIONAL DESCRIPTION

The EMC1462 is an SMBus temperature sensor with a Hardware Thermal Shutdown feature. The EMC1462 monitors one internal diode and one externally connected temperature diode.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the EMC1462 and using that data to control the speed of one or more fans.

The EMC1462 has two levels of monitoring. The first level provides a maskable ALERT signal to the host when the measured temperatures meet or exceed user-programmable limits. This allows the EMC1462 to be used as an independent thermal watchdog to warn the host of temperature hot spots without direct control by the host. The second level of monitoring provides a non-maskable interrupt on the $\overline{\text{THERM}}$ pin if the measured temperatures meet or exceed a second programmable limit.

Figure 4-1 shows a system-level block diagram of the EMC1462

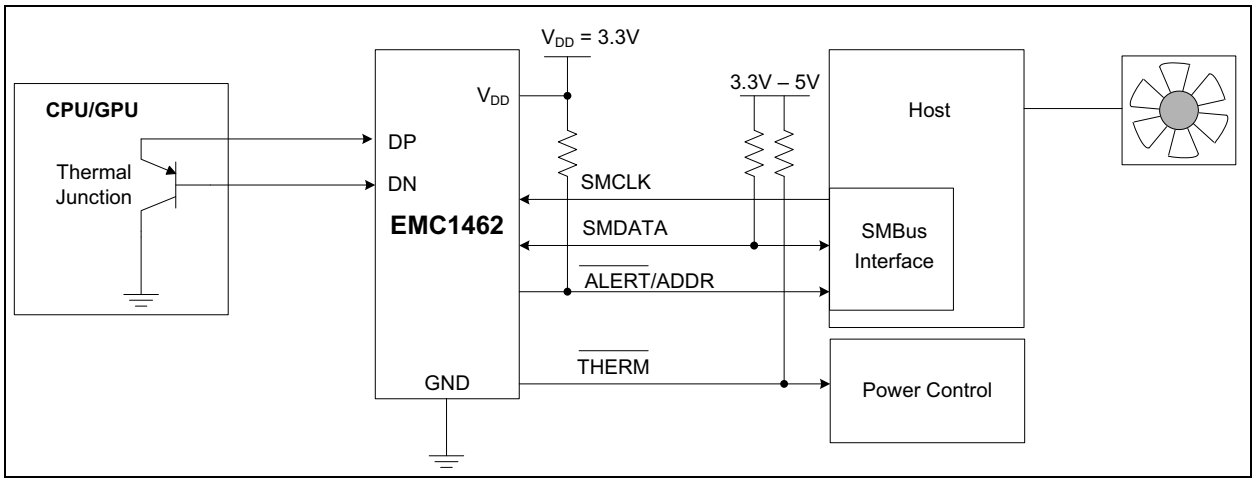


FIGURE 4-1: *EMC1462 - System-Level Block Diagram.*

4.1 Power States

The EMC1462 has two power states.

- Active (Run) – In this state, the ADC converts on all temperature channels at the programmed conversion rate. The temperature data is updated at the end of every conversion, and the limits are checked. In the Active state, writing to the One-Shot register will do nothing.
- Standby (Stop) – In this state, the majority of circuitry is powered down to reduce supply current. The temperature data is not updated, and the limits are not checked. The SMBus is fully active, and the part will return requested data. Writing to the One-Shot register will enable the device to update all temperature channels. When all the channels have been updated, the device will return to Standby mode.

4.1.1 CONVERSION RATES

The EMC1462 may be configured for different conversion rates, based on the system requirements. The default conversion rate is four conversions per second.

Other available conversion rates are shown in Table 4-1.

TABLE 4-1: CONVERSION RATE

CONV<3:0>					Conversions per Second
HEX	3	2	1	0	
0h	0	0	0	0	1/16
1h	0	0	0	1	1/8
2h	0	0	1	0	1/4
3h	0	0	1	1	1/2
4h	0	1	0	0	1
5h	0	1	0	1	2
6h	0	1	1	0	4 (default)
7h	0	1	1	1	8
8h	1	0	0	0	16
9h	1	0	0	1	32
Ah	1	0	1	0	64
Bh - Fh	All others				1

4.1.2 DYNAMIC AVERAGING

Dynamic averaging causes the EMC1462 to measure the external diode channels for an extended time, based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see **Section 6.4 "Configuration Registers"**). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 16x longer than the normal 11-bit operation (nominally 21 ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging applies when a one-shot command is issued. The device will perform the desired averaging during the one-shot operation according to the selected conversion rate.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in Table 4-2.

TABLE 4-2: SUPPLY CURRENT VERSUS CONVERSION RATE

Conversion Rate	Average Supply Current		Averaging	
	Enabled (Default)	Disabled	Enabled (Default)	Disabled
1/16/sec	660 µA	430 µA	16x	1x
1/8/sec	660 µA	430 µA	16x	1x
1/4/sec	660 µA	430 µA	16x	1x
1/2/sec	660 µA	430 µA	16x	1x
1/sec	660 µA	430 µA	16x	1x
2/sec	930 µA	475 µA	16x	1x
4/sec (default)	950 µA	510 µA	8x	1x
8/sec	1010 µA	630 µA	4x	1x
16/sec	1020 µA	775 µA	2x	1x
32/sec	1050 µA	1050 µA	1x	1x
64/sec	1100 µA	1100 µA	0.5x	0.5x

4.2 $\overline{\text{ALERT}}$ Output

The $\overline{\text{ALERT}}$ pin is an open drain output. It requires a pull-up resistor to V_{DD}. The $\overline{\text{ALERT}}$ pin has two modes of operation:

- Interrupt mode
- Comparator mode

The mode of the $\overline{\text{ALERT}}$ output is selected via the ALERT/COMP bit in the Configuration register (see **Section 6.4 "Configuration Registers"**).

4.2.1 $\overline{\text{ALERT}}$ 4

When configured to operate in Interrupt mode, the $\overline{\text{ALERT}}$ pin asserts low when an out-of-limit measurement (> high limit or < low limit) is detected on any diode, or when a diode fault is detected. The $\overline{\text{ALERT}}$ pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the $\overline{\text{ALERT}}$ pin will remain asserted until the appropriate status bits are cleared.

The $\overline{\text{ALERT}}$ pin can be masked by setting the MASK_ALL bit. Once the $\overline{\text{ALERT}}$ pin has been masked, it will be deasserted and remain deasserted until the MASK_ALL bit is cleared by the user. Any interrupt conditions that occur while the $\overline{\text{ALERT}}$ pin is masked will update the Status register normally. There are also individual channel masks (see **Section 6.11 "Consecutive ALERT Register"**).

The $\overline{\text{ALERT}}$ pin is used as an interrupt signal or as an SMBus Alert signal that allows an SMBus target to communicate an error condition to the master. One or more ALERT outputs can be hardwired together.

4.2.2 $\overline{\text{ALERT}}$ PIN COMPARATOR MODE

When the $\overline{\text{ALERT}}$ pin is configured to operate in Comparator mode, it will be asserted if any of the measured temperatures exceeds the respective high limit. The $\overline{\text{ALERT}}$ pin will remain asserted until all temperatures drop below the corresponding high limit minus the Therm Hysteresis value.

When the $\overline{\text{ALERT}}$ pin is asserted in Comparator mode, the corresponding high-limit status bits will be set. Reading these bits will not clear them until the $\overline{\text{ALERT}}$ pin is deasserted. When the ALERT pin is deasserted, the status bits will be cleared automatically.

The MASK_ALL bit will not block the $\overline{\text{ALERT}}$ pin in this mode. However, the individual channel masks (see **Section 6.10 "Channel Mask Register"**) will prevent the respective channel from asserting the $\overline{\text{ALERT}}$ pin.

4.2.3 $\overline{\text{ALERT}}$ PIN CONSIDERATIONS

Because of the decode method that is used to determine the SMBus Address, it is important that the pull-up resistance on $\overline{\text{ALERT}}$ pin is within ±10% tolerance. Additionally, the pull-up resistor on the $\overline{\text{ALERT}}$ pin must be connected to the same 3.3V supply that drives the VDD pin.

For 15 ms after power-up, the $\overline{\text{ALERT}}$ pin must not be pulled low, or the SMBus Address will not be decoded properly. If the system requirements do not permit these conditions, the $\overline{\text{ALERT}}$ pin must be isolated from the bus during this time.

The digital block shall wait 10 ms before initiating the $\overline{\text{ALERT}}$ decode.

One method of isolating this pin is shown in Figure 4-2.

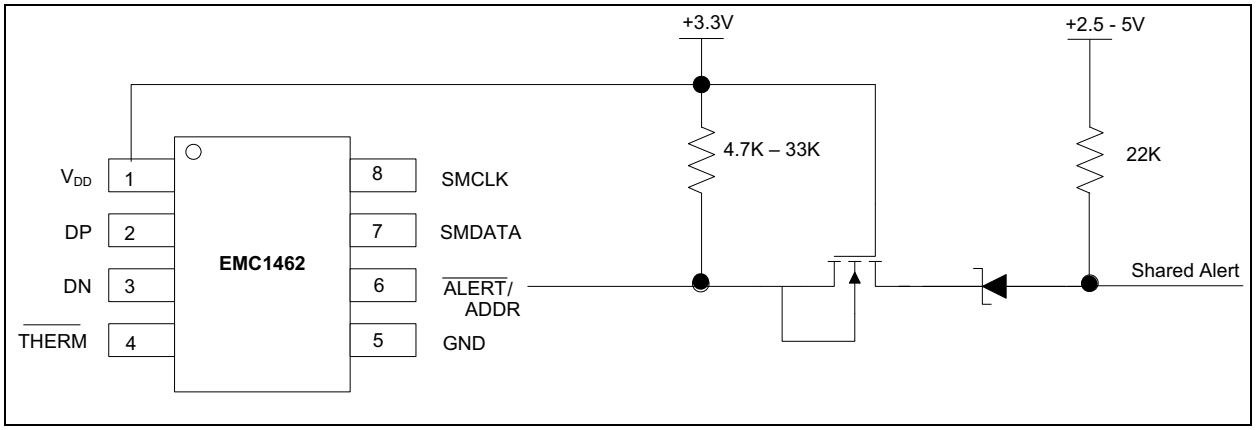


FIGURE 4-2: *Isolating the ALERT Pin.*

4.3 Temperature Measurement

The EMC1462 can monitor the temperature of up to 3 externally connected diodes.

The device contains programmable high, low and therm limits for all measured temperature channels. If the measured temperature goes below the low limit or above the high limit, the ALERT pin can be asserted (based on user settings). If the measured temperature meets or exceeds the therm limit, the THERM pin is asserted unconditionally, providing two tiers of temperature detection.

4.3.1 BETA COMPENSATION

The EMC1462 is configured to monitor the temperature of basic diodes (e.g., 2N3904) or CPU thermal diodes. For External Diode 1, it automatically detects the type of external diode (CPU diode or diode-connected transistor) and determines the optimal setting to reduce temperature errors introduced by beta variation. Compensating for this error is also known as implementing the transistor or BJT model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However, for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause a large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

4.3.2 RESISTANCE ERROR CONNECTION (REC)

Parasitic resistance in series with the external diodes will limit the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents causes the temperature measurement to read higher than the true temperature. Contributors to series resistance are PCB trace resistance, on die (i.e., on the processor) metal resistance or bulk resistance in the base and emitter of the temperature transistor. Typically, the error caused by series resistance is +0.7°C per ohm. The EMC1462 automatically corrects up to 100 ohms of series resistance.

4.3.3 PROGRAMMABLE EXTERNAL DIODE IDEALITY FACTOR

The EMC1462 is designed for external diodes with an ideality factor of 1.008. Not all external diodes, processor or discrete, will have this exact value. This variation of the ideality factor introduces error in the temperature measurement that must be corrected. This correction is typically achieved using programmable offset registers. Since an ideality factor mismatch introduces an error that is a function of temperature, this correction is only accurate within a small range of temperatures. To provide maximum flexibility to the user, the EMC1462 provides a 6-bit register for each external diode where the ideality factor of the diode used is programmed to eliminate errors across all temperatures.

Note 1:	When monitoring a substrate transistor or CPU diode, and beta compensation is enabled, the ideality factor should not be adjusted.
2:	Beta compensation automatically corrects for most ideality errors.

4.4 Diode Faults

The EMC1462 detects an open on the DP and DN pins and a short across the DP and DN pins. For each temperature measurement made, the device checks for a diode fault on the external diode channel(s). When a diode fault is detected, the ALERT pin asserts (unless masked, see **Section 4.5 "Consecutive Alerts"**), and the temperature data reads 00h in the MSB and LSB registers. Note that the low limit will not be checked. A diode fault is defined as one of the following:

- An Open Between DP and DN
- A Short From V_{DD} to DP
- A Short From V_{DD} to DN

If a short occurs across DP and DN, or a short occurs from DP to GND, the low-limit status bit is set and the ALERT pin asserts (unless masked). This condition is indistinguishable from a temperature measurement of 0.000°C (-64°C in extended range), resulting in temperature data of 00h in the MSB and LSB registers.

If a short from DN to GND occurs (with a diode connected), temperature measurements will continue as normal with no alerts.

4.5 Consecutive Alerts

The EMC1462 contains multiple consecutive alert counters.

- One Shared Counter for the ALERT and THERM Signals
- One Counter for the ALERT Signal
- One Counter for the THERM Signal

Each temperature measurement channel has a separate consecutive alert counter for each of the ALERT and THERM pins. All counters are user programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit, or reporting a diode fault, before the corresponding pin is asserted.

See Register 6-8 for more details on the consecutive alert function.

The default setting is one consecutive out-of-limit conversion, as shown in Table 4-3, and is set in the CONSEC ALERT register.

When a value that is not defined in Table 4-3 is written to Register 6-8, the command is ignored and the last valid value is maintained.

TABLE 4-3: CONSECUTIVE ALERT/THERM SETTINGS

2	1	0	Number of Consecutive Out-of-Limit Measurements
0	0	0	1 (default for CALRT<2:0>)
0	0	1	2
0	1	1	3
1	1	1	4 (default for CTHRM<2:0>)

4.6 Digital Filter

To save on complexity, the digital filter will only apply to the External Diode 1 channel. It will apply after the digital block has taken the appropriate 11-bits, based on the dynamic averaging.

To reduce the effect of noise and temperature spikes on the reported temperature, the External Diode 1 channel uses a programmable digital filter. This filter can be configured as Level 1, Level 2 or Disabled (default). The typical filter performance is shown in Figure 4-3 and Figure 4-4.

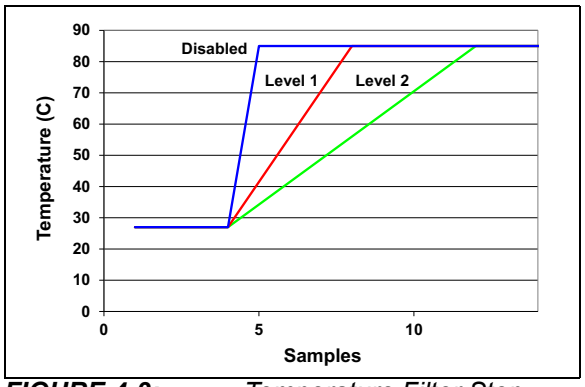


FIGURE 4-3: *Temperature Filter Step Response.*

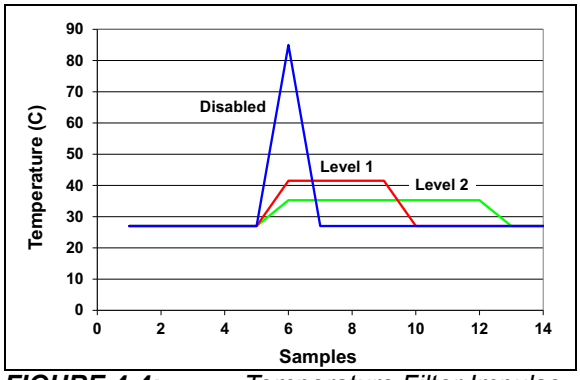


FIGURE 4-4: *Temperature Filter Impulse Response.*

4.7 Temperature Measurement Results and Data

The temperature measurement results are stored in the internal and external temperature registers. These are compared with the values stored in the high and low limit registers. Both external and internal temperature measurements are stored in 11-bit format with the 8 MSb stored in a high byte register and the 3 LSb stored in the 3 MSb positions of the low byte register. All other bits of the low byte register are set to zero.

The EMC1462 has two selectable temperature ranges. The default range is from 0°C to +127°C and the temperature is represented as a binary number that is able to report a temperature from 0°C to +127.875°C in 0.125°C steps.

The extended temperature range is from -64°C to +191°C. The data format is a binary number offset by 64°C. The extended range is used to measure temperature diodes with a large known offset (such as AMD processor diodes) where the diode temperature, plus the offset, would be equivalent to a temperature higher than +127°C.

Table 4-4 shows the default and extended range formats.

TABLE 4-4: TEMPERATURE DATA FORMAT

Temperature (°C)	Default Range 0°C to +127°C	Extended Range -64°C to +191°C
Diode Fault	000 0000 0000	000 0000 0000
-64	000 0000 0000	000 0000 0000 (**Note 2**)
-1	000 0000 0000	001 1111 1000
0	000 0000 0000 (**Note 1**)	010 0000 0000
0.125	000 0000 0001	010 0000 0001
1	000 0000 1000	010 0000 1000
64	010 0000 0000	100 0000 0000
65	010 0000 1000	100 0000 1000
127	011 1111 1000	101 1111 1000
127.875	011 1111 1111	101 1111 1111
128	011 1111 1111 (**Note 3**)	110 0000 0000
190	011 1111 1111	111 1111 0000
191	011 1111 1111	111 1111 1000
≥ 191.875	011 1111 1111	111 1111 1111 (**Note 4**)

Note 1: In the default range, all temperatures below 0°C are reported as 0°C.

2: In the extended range, all temperatures below -64°C are reported as -64°C.

3: For the default range, all temperatures above +127.875°C are reported as +127.875°C.

4: For the extended range, all temperatures above +191.875°C are reported as +191.875°C.

4.8 External Diode Connections

The EMC1462 can be configured to measure a CPU substrate transistor, a discrete 2N3904 thermal diode, or an AMD processor diode.

The diodes can be connected as indicated in the two examples in Figure 4-5.

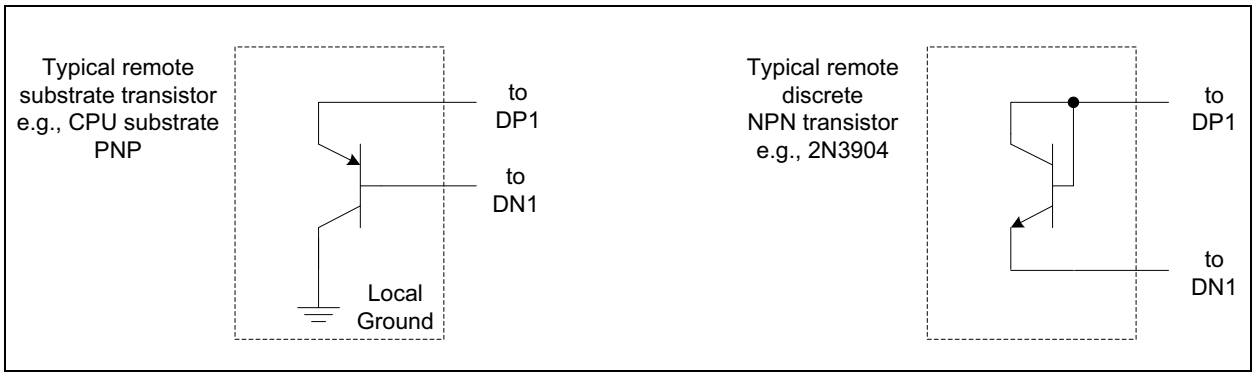


FIGURE 4-5: *Diode Configurations.*

5.0 SYSTEM MANAGEMENT BUS PROTOCOL

5.1 Communications Protocol

The EMC1462 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 5-1.

For the first 15 ms after power-up, the device may not respond to SMBus communications.

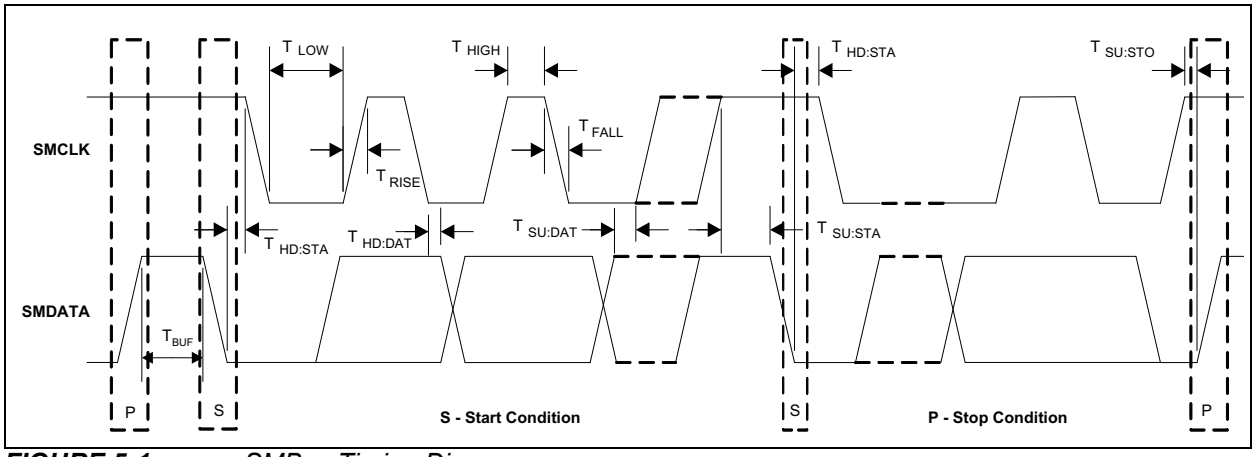


FIGURE 5-1: *SMBus Timing Diagram.*

5.1.1 SMBUS START BIT

The SMBus Start bit is defined as a transition of the SMBus data line from a logic '1' state to a logic '0' state, while the SMBus clock line is in a logic '1' state.

5.1.2 SMBUS ADDRESS AND RD/$\overline{WR}$ BIT

The SMBus Address byte consists of the 7-bit client address followed by the RD/WR indicator bit. If this RD/WR bit is a logic '0', the SMBus host is writing data to the client device. If this RD/WR bit is a logic '1', the SMBus Host is reading data from the client device.

The address decode is performed by pulling known currents from V_{DD} through the external resistor (causing the pin voltage to drop), based on the respective current/resistor relationship. This pin voltage is compared against a threshold that determines the value of the pull-up resistor.

The EMC1462 SMBus target address is determined by the pull-up resistor on the $\overline{ALERT}$ pin as shown in Table 5-1.

TABLE 5-1: SMBUS ADDRESS DECODE

$\overline{ALERT}$ Pin Pull-Up Resistor (±5%)	I^2C 7-bit Target Address
4.7k	1111_100(r/w)b
6.8k	1011_100(r/w)b
10k	1001_100(r/w)b
15k	1101_100(r/w)b
22k	0011_100(r/w)b
33k	0111_100(r/w)b

5.1.3 ALERT PIN CONSIDERATIONS

Because of the decode method used to determine the SMBus address, it is important that the pull-up resistance on the ALERT pin is within the tolerances shown in Table 5-1. Additionally, the pull-up resistor on the ALERT pin must be connected to the same 3.3V supply that drives the VDD pin.

For 15 ms after power-up, the ALERT pin must not be pulled low, or the SMBus address will not be decoded properly. If the ALERT requirements do not permit this condition, the ALERT pin must be isolated from its hardwired OR'd bus during this time.

The digital block shall wait 15 ms before initiating the ALERT decode.

One method of isolating this pin is shown in Figure 5-2.

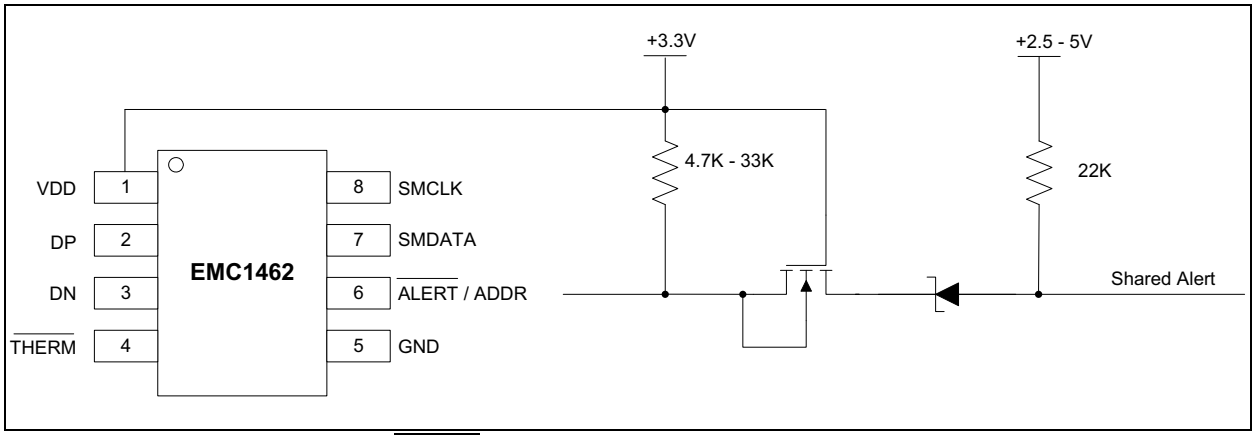


FIGURE 5-2: *Isolating the ALERT Pin.*

5.1.4 SMBUS DATA BYTES

All SMBus data bytes are sent MSb first, and composed of 8 bits of information.

5.1.5 SMBUS ACK AND NACK BITS

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus data line low after the 8th bit of each byte that is transmitted. This applies to the Write Byte protocol.

The host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent.

5.1.6 SMBUS STOP BIT

The SMBus Stop bit is defined as a transition of the SMBus data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the device detects an SMBus Stop bit and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

5.1.7 SMBUS TIME-OUT

The EMC1462 supports SMBus Timeout. If the clock line is held low for longer than TIMEOUT, the device will reset its SMBus protocol. This function can be enabled by setting the TIMEOUT bit, see Register 6-8.

5.1.8 SMBUS AND I²C COMPLIANCE

The EMC1462 is compatible with SMBus and I²C. The major differences between SMBus and I²C devices are:

- EMC1462 supports I²C fast mode at 400 kHz. This covers the SMBus max. time of 100 kHz.
- Minimum frequency for SMBus communications is 10 kHz.
- The SMBus client protocol resets if the clock is held at a logic '0' for longer than 30 ms. This time-out functionality is disabled by default in the EMC1462 and can be enabled by writing to the TIMEOUT bit. I²C does not have a time-out.
- I²C devices do not support the Alert Response Address functionality (which is optional for SMBus).

Attempting to communicate with the EMC1462 SMBus interface with an invalid target address or invalid protocol will result in no response from the device and will not affect its register contents. Stretching of the SMCLK signal is supported, provided that other devices on the SMBus control the timing.

For more information, refer to the SMBus 2.0 and I²C specifications. For information on using the EMC1462 in an I²C system, refer to *Application Note 14.0 Microchip Dedicated Slave Devices in I²C™ Systems* (DS00001853).

5.2 SMBus Protocols

The EMC1462 is SMBus v.2.0 compatible and supports Send Byte, Read Byte, Block Read and Receive Byte as valid protocols, as shown in this section. The EMC1462 also supports the I^2C Block Read and Block Write protocols. The device supports Write Byte, Read Byte and Block Read/Block Write.

All the protocols described in this section use the convention in Table 5-2.

TABLE 5-2: SMBUS PROTOCOL FORMAT

Data Sent to Device	Data Sent to Host
# of bits sent	# of bits sent

5.2.1 WRITE BYTE PROTOCOL

The Write Byte protocol is used to write one byte of data to a specific register, as shown in Table 5-3.

TABLE 5-3: SMBUS WRITE BYTE PROTOCOL

START	Target Address	WR	ACK	Register Address	ACK	Register Data	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 → 1

5.2.2 BLOCK WRITE PROTOCOL

The Block Write protocol is used to write multiple data bytes to a group of contiguous registers, as shown in Table 5-4. It is an extension of the Write Byte Protocol.

TABLE 5-4: SMBUS BLOCK WRITE PROTOCOL

START	Target Address	WR	ACK	Register Address	ACK	Repeat N Times		STOP
						Register Data	ACK	
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 → 1

5.2.3 READ BYTE PROTOCOL

The Read Byte protocol is used to read one byte of data from the registers, as shown in Table 5-5.

TABLE 5-5: SMBUS READ BYTE PROTOCOL

START	Target Address	WR	ACK	Register Address	ACK	
1 → 0	YYYY_YYY	0	0	XXh	0	
START	**Target Address**	**RD**	**ACK**	**Register Data**	**NACK**	**STOP**
1 → 0	0101_000	1	0	XXh	1	0 → 1

5.2.4 BLOCK READ PROTOCOL

The Block Read protocol is used to read multiple data bytes from a group of contiguous registers, as shown in Table 5-6. It is an extension of the Read Byte Protocol.

TABLE 5-6: SMBUS BLOCK READ PROTOCOL

START	Target Address	WR	ACK	Register Address	ACK			
1 → 0	YYYY_YYY	0	0	XXh	0			
START	**Target Address**	**RD**	**ACK**	**Register Data**	**ACK**	**Register Data**	**NACK**	**STOP**
1 → 0	YYYY_YYY	1	0	XXh	0	XXh	1	0 → 1

5.2.5 SEND BYTE PROTOCOL

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol, as shown in Table 5-7.

TABLE 5-7: SMBUS SEND BYTE PROTOCOL

START	Target Address	WR	ACK	Register Address	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	0 → 1

5.2.6 RECEIVE BYTE PROTOCOL

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g., set via Send Byte). This is used for consecutive reads of the same register, as shown in Table 5-8.

TABLE 5-8: SMBUS RECEIVE BYTE PROTOCOL

START	Target Address	RD	ACK	Register Data	NACK	STOP
1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

5.3 Alert Response Addresses (ARA)

The ALERT output can be used as a processor interrupt or as an SMBus Alert.

When it detects that the ALERT pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in Table 5-9.

TABLE 5-9: SMBUS ALERT RESPONSE ADDRESS PROTOCOL

Start	Alert Response Address	RD	ACK	Device Address	NACK	Stop
1 → 0	0001_100	1	0	YYYY_YYY	1	0 → 1

The EMC1462 responds to the ARA in the following way:

- Send the Target Address and verify that the full target address was sent (for example, the SMBus communication from the device was not prematurely stopped due to a bus contention event).
- Set the MASK_ALL bit to clear the $\overline{\text{ALERT}}$ pin.

Note: The ARA does not clear the Status register. If the MASK_ALL bit is cleared prior to the Status register being cleared, the $\overline{\text{ALERT}}$ pin will be reasserted.

6.0 REGISTER DESCRIPTION

The registers shown in Table 6-1 are accessible through the SMBus. An entry of '—' indicates that the bit is not used and will always read '0'.

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER

Register Address	Register / Table #	Register Name	R/W	Function	Default (POR) Value
00h	Register 6-1	Internal Diode High Byte	R	Stores the integer data for the internal diode.	00h
01h	Register 6-1	External Diode High Byte	R	Stores the integer data for the external diode.	00h
02h	Register 6-2	Status	R/W: R/C	Reports the operating status of the internal diode and external diode channels	00h
03h	Register 6-3	Configuration	R/W	Controls the general operation of the device (mirrored at address 09h).	00h
04h	Register 6-4	Conversion Rate	R/W	Controls the conversion rate for updating temperature data (mirrored at address 0Ah).	06h (4/sec)
05h	Table 6-2	Internal Diode High Limit	R/W	Stores the 8-bit high limit for the internal diode (mirrored at address 0Bh).	55h (85°C)
06h	Table 6-2	Internal Diode Low Limit	R/W	Stores the 8-bit low limit for the internal diode (mirrored at address 0Ch).	00h (0°C)
07h	Table 6-2	External Diode High Limit High Byte	R/W	Stores the integer portion of the high limit for the external diode (mirrored at register 0Dh).	55h (85°C)
08h	Table 6-2	External Diode Low Limit High Byte	R/W	Stores the integer portion of the low limit for the external diode (mirrored at register 0Eh).	00h (0°C)
09h	Register 6-3	Configuration	R/W	Controls the general operation of the device (mirrored at address 03h).	00h
0Ah	Register 6-4	Conversion Rate	R/W	Controls the conversion rate for updating temperature data (mirrored at address 04h).	06h (4/sec)
0Bh	Table 6-2	Internal Diode High Limit	R/W	Stores the 8-bit high limit for the internal diode (mirrored at address 05h).	55h (85°C)
0Ch	Table 6-2	Internal Diode Low Limit	R/W	Stores the 8-bit low limit for the internal diode (mirrored at address 06h).	00h (0°C)
0Dh	Table 6-2	External Diode High Limit High Byte	R/W	Stores the integer portion of the high limit for the external diode (mirrored at register 07h).	55h (85°C)
0Eh	Table 6-2	External Diode Low Limit High Byte	R/W	Stores the integer portion of the low limit for the external diode (mirrored at register 08h).	00h (0°C)
0Fh	Register 6-6	One Shot	W	Initiates a one shot command.	—
10h	Register 6-1	External Diode Low Byte	R	Stores the fractional data for the external diode.	00h
11h	Register 6-5	Scratchpad	R/W	Scratchpad register for software compatibility	00h
12h	Register 6-5	Scratchpad	R/W	Scratchpad register for software compatibility	00h
13h	Table 6-2	External Diode High Limit Low Byte	R/W	Stores the fractional portion of the high limit for external diode.	00h
14h	Table 6-2	External Diode Low Limit Low Byte	R/W	Stores the fractional portion of the low limit for external diode.	00h
19h	Table 6-3	External Diode Therm Limit	R/W	Stores the 8-bit critical temperature limit for external diode.	7Dh (125°C)

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Address	Register / Table #	Register Name	R/W	Function	Default (POR) Value
1Fh	Register 6-7	Channel Mask	R/W	Controls the masking of individual channels.	00h
20h	Table 6-3	Internal Diode Therm Limit	R/W	Stores the 8-bit critical temperature limit for the internal diode.	7Dh (125°C)
21h	Table 6-3	Therm Hysteresis	R/W	Stores the 8-bit hysteresis value that applies to all Therm limits.	0Ah (10°C)
22h	Register 6-8	Consecutive ALERT	R/W	Controls the number of out-of-limit conditions that must occur before an interrupt is asserted.	70h
25h	Register 6-9	Beta Configuration	R/W	Stores the Beta Compensation circuitry settings for the external diode.	08h
27h	Register 6-10	External Diode Ideality Factor	R/W	Stores the ideality factor for the external diode.	12h (1.008)
29h	Register 6-1	Internal Diode Low Byte	R	Stores the fractional data for the internal diode.	00h
40h	Register 6-11	Filter Configuration	R/W	Controls the digital filter setting for the external diode channel.	00h
FDh	Register 6-12	Product ID	R	Stores a fixed value that identifies the device.	60h
FEh	Register 6-13	Manufacturer ID	R	Stores a fixed value that represents Microchip.	5Dh
FFh	Register 6-14	Revision	R	Stores a fixed value that represents the revision number.	06h

6.1 Data Read Interlock

When any temperature channel high byte register is read, the corresponding low byte is copied into an internal ‘shadow’ register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte.

Whether the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

6.2 Temperature Data Registers

As shown in Register 6-1, all temperatures are stored as an 11-bit value with the high byte representing the integer value and the low byte (representing the fractional value) left justified to occupy the MSbs.

REGISTER 6-1: TEMPERATURE DATA REGISTERS (ADDRESSES 00h/29h/01h/10h)

Register Address	R/W	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
00h	R	Internal Diode High Byte	128	64	32	16	8	4	2	1	00h
29h	R	Internal Diode Low Byte	0.5	0.25	0.125	—	—	—	—	—	00h
01h	R	External Diode High Byte	128	64	32	16	8	4	2	1	00h
10h	R	External Diode Low Byte	0.5	0.25	0.125	—	—	—	—	—	00h

6.3 Status Register

The Status Register reports the operating status of the Internal Diode and External Diode channels. When any of the bits are set (excluding the BUSY bit), either the ALERT or THERM pin is asserted.

The ALERT and THERM pins are controlled by the respective consecutive alert counters (see Section 6.11) and will not be asserted until the programmed consecutive alert count has been reached.

The status bits (except ETHERM and ITHERM) will remain set until read, unless the ALERT pin is configured as a second THERM output (see **Section 4.2.2 "ALERT Pin Comparator Mode"**).

REGISTER 6-2: STATUS REGISTER (ADDRESS 02h)

R-C	R-C	R-C	R-C	R-C	R-C	R-C	R-C
BUSY	IHIGH	ILOW	EHIGH	ELOW	FAULT	ETHERM	ITHERM
bit 7							bit 0

Legend:			
R = Readable bit	R-C = Read - Clear	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **BUSY:** Indicates that the ADC is currently converting. This bit does not cause either the ALERT or THERM pin to be asserted.
1 = Converter busy.
0 = Converter idle. (Default)

bit 6 **IHIGH**: This bit is set when the Internal Diode channel exceeds its programmed high limit.
1 = High limit exceeded.
0 = High limit not exceeded. (Default)

bit 5 **ILOW**: This bit is set when the Internal Diode channel drops below its programmed low limit. When set, this bit will assert the ALERT pin.
1 = Low limit exceeded.
0 = Low limit not exceeded. (Default)

bit 4 **EHIGH**: This bit is set when the External Diode channel exceeds its programmed high limit. When set, this bit will assert the ALERT pin.
1 = Low limit exceeded.
0 = Low limit not exceeded. (Default)

bit 3 **ELOW**: This bit is set when the External Diode channel drops below its programmed low limit. When set, this bit will assert the ALERT pin.
1 = Low limit exceeded.
0 = Low limit not exceeded. (Default)

bit 2 **FAULT**: This bit is asserted when a diode fault is detected. When set, this bit will assert the ALERT pin.
1 = Diode fault detected.
0 = Diode fault not detected. (Default)

bit 1 **ETHERM**: This bit is set when the External Diode channel exceeds the programmed Therm Limit. When set, this bit will assert the THERM pin. This bit will remain set until the THERM pin is released, at which point it will be automatically cleared.
1 = Therm limit exceeded.
0 = Therm limit not exceeded. (Default)

bit 0 **ITHERM**: This bit is set when the Internal Diode channel exceeds the programmed Therm Limit. When set, this bit will assert the THERM pin. This bit will remain set until the THERM pin is released, at which point it will be automatically cleared.
1 = Therm limit exceeded.
0 = Therm limit not exceeded. (Default)

6.4 Configuration Registers

The Configuration Registers control the basic operation of the device. This register is fully accessible at either address.

REGISTER 6-3: CONFIGURATION REGISTERS (ADDRESSES 03h/09h)

R/W-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
MASK_ALL	RUN/STOP	ALERT/COMP	RECD1	—	RANGE	DAVG_DIS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **MASK_ALL**: Masks the $\overline{\text{ALERT}}$ pin from asserting.
- 1 = The $\overline{\text{ALERT}}$ pin is masked. It will not be asserted for any interrupt condition unless it is configured in Comparator mode. The Status registers will be updated normally. (Default)
- 0 = The $\overline{\text{ALERT}}$ pin is not masked. If any of the appropriate status bits are set, the $\overline{\text{ALERT}}$ pin will be asserted.

bit 6 **RUN/STOP**: Controls Active/Standby modes.
- 1 = The device is in Standby mode and not converting.
- 0 = The device is in Active mode and converting on all channels. (Default)

bit 5 **ALERT/COMP:** Controls the operation of the $\overline{\text{ALERT}}$ pin.
- 1 = The $\overline{\text{ALERT}}$ pin acts in Comparator mode, as described in Section 5.2.2. In this mode, the MASK_ALL bit is ignored.
- 0 = The $\overline{\text{ALERT}}$ pin acts as described in Section 5.2. (Default)

bit 4 **RECD1**: Disables the Resistance Error Correction (REC) for the External Diode 1.
- 1 = REC is disabled for the External Diode 1.
- 0 = REC is enabled for the External Diode 1. (Default)

bit 3 **Unimplemented**: Read as '0'.

bit 2 **RANGE**: Configures the measurement range and data format of the temperature channels.
- 1 = The temperature measurement range is -64°C to +191.875°C and the data format is offset binary (see Table 5.2).
- 0 = The temperature measurement range is 0°C to +127.875°C and the data format is binary. (Default)

bit 1 **DAVG_DIS:** Disables the dynamic averaging feature on all temperature channels.
- 1 = The dynamic averaging feature is disabled. All temperature channels will be converted with a maximum averaging factor of 1x (equivalent to 11-bit conversion). For higher conversion rates, this averaging factor will be reduced.
- 0 = (default) The dynamic averaging feature is enabled. All temperature channels will be converted with an averaging factor that is based on the conversion rate.

bit 0 **Unimplemented**: Read as '0'.

6.5 Conversion Rate Registers

The Conversion Rate Registers control how often the temperature measurement channels are updated and compared against the limits. This register is fully accessible at either address.

REGISTER 6-4: CONVERT – TEMPERATURE CONVERSION RATE REGISTERS (ADDRESSES 04h/ 0Ah)

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	CONV<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented**: Read as ‘0’.

bit 3-0 **CONV<3:0>**: Determines the conversion rate, as shown in Table 4-1.

6.6 Limit Registers

The device contains both high and low limits for all temperature channels. If the measured temperature exceeds the high limit, then the corresponding status bit is set and the ALERT pin is asserted. Likewise, if the measured temperature is less than or equal to the low limit, the corresponding status bit is set and the ALERT pin is asserted.

The data format for the limits must match the selected data format for the temperature so that if the extended temperature range is used, the limits must be programmed in the extended data format.

The limit registers with multiple addresses are fully accessible at either address.

When the device is in Standby mode, updating the limit registers will have no effect until the next conversion cycle occurs. This can be initiated via a write to the One Shot register (see **Section 6.8 "One Shot Register"**) or by clearing the RUN/STOP bit (see **Section 6.4 "Configuration Registers"**).

TABLE 6-2: TEMPERATURE LIMIT REGISTERS

Register Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
05h 0Bh	Internal Diode High Limit	R/W	128	64	32	16	8	4	2	1	55h (85°C)
06h 0Ch	Internal Diode Low Limit	R/W	128	64	32	16	8	4	2	1	00h (0°C)
07h 0Dh	External Diode High Limit High Byte	R/W	128	64	32	16	8	4	2	1	55h (85°C)
13h	External Diode High Limit Low Byte	R/W	0.5	0.25	0.125	—	—	—	—	—	00h
08h 0Eh	External Diode Low Limit High Byte	R/W	128	64	32	16	8	4	2	1	00h (0°C)
14h	External Diode Low Limit Low Byte	R/W	0.5	0.25	0.125	—	—	—	—	—	00h

6.7 Scratchpad Registers

REGISTER 6-5: SCRATCHPAD REGISTERS (ADDRESSES 11h /12h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **SPD<7:0>:** The Scratchpad registers are Read/Write registers that are used for place holders to be software compatible with legacy programs. Reading from the registers will return what is written to them.

6.8 One Shot Register

REGISTER 6-6: ONE SHOT REGISTER (ADDRESS 0Fh)

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
ONSH<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ONSH<7:0>:**The One Shot Register is used to initiate a one shot command. Writing to the one shot register when the device is in Standby mode, and the BUSY bit (in Status Register) is '0', will immediately cause the ADC to update all temperature measurements. Writing to the One Shot register while the device is in Active mode will have no effect.

6.9 Therm Limit Registers

The Therm Limit Registers are used to determine whether a critical thermal event has occurred. If the measured temperature exceeds the Therm Limit, the $\overline{\text{THERM}}$ pin is asserted. The limit setting must match the chosen data format of the temperature reading registers.

Unlike the $\overline{\text{ALERT}}$ pin, the $\overline{\text{THERM}}$ pin cannot be masked. Additionally, the $\overline{\text{THERM}}$ pin will be released once the temperature drops below the corresponding threshold minus the Therm Hysteresis.

TABLE 6-3: THERM LIMIT REGISTERS (ADDRESSES 19h/20h/21h)

Register Address	Register Name	R/W	Bit 7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
19h	External Diode Therm Limit	R/W	128	64	32	16	8	4	2	1	7Dh (125°C)
20h	Internal Diode Therm Limit	R/W	128	64	32	16	8	4	2	1	7Dh (125°C)
21h	Therm Hysteresis	R/W	128	64	32	16	8	4	2	1	0Ah (10°C)

6.10 Channel Mask Register

The Channel Mask Register controls individual channel masking. If a channel is masked and it reads a diode fault or an out-of-limit error, the $\overline{\text{ALERT}}$ pin will not be asserted. The channel mask does not mask the $\overline{\text{THERM}}$ pin.

REGISTER 6-7: CHANNEL MASK REGISTER (ADDRESS 1Fh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	EXTMSK	INTMSK
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented**: Read as ‘0’.

bit 1 **EXTMSK:** Masks the $\overline{\text{ALERT}}$ pin from asserting when the External Diode channel is out-of-limit or reports a diode fault.

1 = The External Diode 1 channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit or reports a diode fault.

0 = The External Diode channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit or reports a diode fault. (Default)

bit 0 **INTMSK:** Masks the $\overline{\text{ALERT}}$ pin from asserting when the Internal Diode temperature is out-of-limit.

1 = The Internal Diode channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit.

0 = The Internal Diode channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit.

6.11 Consecutive ALERT Register

The Consecutive ALERT Register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the ALERT or THERM pin is asserted. Additionally, the Consecutive ALERT Register controls the SMBus Timeout functionality.

An out-of-limit condition (i.e. HIGH, LOW or FAULT) occurring on the same temperature channel in consecutive measurements will increment the consecutive alert counter. The counters will also be reset if an out-of-limit condition or diode fault condition does not occur in a consecutive reading.

If the ALERT pin is configured as an interrupt, when the consecutive alert counter reaches its programmed value, the STATUS bit(s) for that channel and the last error condition(s) (i.e., E1HIGH) will be set to '1', the ALERT pin will be asserted, the consecutive alert counter will be cleared and measurements will continue.

If the ALERT pin is configured as a comparator, the consecutive alert counter will ignore diode fault and low limit errors and only increment if the measured temperature exceeds the high limit. Additionally, once the consecutive alert counter reaches the programmed limit, the ALERT pin will be asserted, but the counter will not be reset. It will remain set until the temperature drops below the high limit minus the Therm Hysteresis value.

REGISTER 6-8: CONSECUTIVE ALERT REGISTER (ADDRESS 22h)

R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	U-0
TMOUT	CTHRM<2:0>			CALRT<2:0>			—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TMOUT:** Determines the time-out functionality of the SMBus protocol.

1 = The SMBus Time-out feature is enabled. If the SMCLK line is held low for more than TIMEOUT, the device will reset the SMBus protocol.

0 = The SMBus Time-out feature is disabled. The SMCLK line can be held low indefinitely without the device resetting its SMBus protocol (default).

bit 6-4 **CTHRM<2:0>:** Determines the number of consecutive measurements that must exceed the corresponding Therm Limit before the THERM pin is asserted. All temperature channels use this value to set the respective counters. The consecutive Therm counter is incremented whenever any measurement exceeds the corresponding Therm Limit.

If the temperature drops below the Therm Limit, the counter is reset. If a number of consecutive measurements above the Therm Limit occurs, the THERM pin is asserted low.

When the THERM pin has been asserted, the consecutive therm counter will not reset until the corresponding temperature drops below the Therm Limit minus the Therm Hysteresis value.

The bits are decoded as shown in Table 6-4. The default setting is four consecutive out-of-limit conversions.

000 = 1
001 = 2
011 = 3
111 = 4

bit 3-1 **CALRT<2:0>:** Determine the number of consecutive measurements that must have an out-of-limit condition or diode fault before the ALERT pin is asserted. Both temperature channels use this value to set the respective counters. The bits are decoded as shown in Table 6-4 The default setting is one consecutive out-of-limit conversion.

000 = 1
001 = 2
011 = 3
111 = 4

bit 0 **Unimplemented:** Read as '0'.

TABLE 6-4: CONSECUTIVE ALERT/THERM SETTINGS

2	1	0	Number of Consecutive Out-of-Limit Measurements
0	0	0	1 (default for CALRT<2:0>)
0	0	1	2
0	1	1	3
1	1	1	4 (default for CTHRM<2:0>)

For example, if the CALRT<2:0> bits are set for four consecutive alerts on an EMC1462 device, the high limits are set at 70°C, and none of the channels are masked. The ALERT pin will be asserted after the following four measurements:

- The internal diode reads 71°C and external diode reads 69°C. Consecutive alert counter for INT is incremented to 1.
- Both the internal diode and the external diode read 71°C. Consecutive alert counter for INT is incremented to 2 and for EXT1 is set to 1.
- The external diode reads 71°C and the Internal Diode reads 69°C. The consecutive alert counters for INT is cleared and EXT is incremented to 2.
- The internal diode reads 71°C and the external diodes reads 71°C. Consecutive alert counter for INT is set to 1 and EXT to 3.
- The internal diode reads 71°C and the external diode reads 71°C. Consecutive alert counter for INT is incremented to 2 and EXT is incremented to 4. The appropriate status bits are set for EXT and the ALERT pin is asserted. The EXT counter is reset to 0 and all other counters hold the last value until the next temperature measurement.

6.12 Beta Configuration Register

This register is used to set the Beta Compensation factor that is used for external diode channels.

REGISTER 6-9: BETA CONFIGURATION REGISTER (ADDRESS 25h)

U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0	R/W-0
—	—	—	—	ENABLE	BETA<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
RC = Read-then-clear bit			

bit 7-4 **Unimplemented**: Read as '0'.

bit 3 **ENABLE:** Enables the Beta Compensation factor auto-detection function for the external diode.

1 = The Beta Compensation factor auto-detection circuitry is enabled. At the beginning of every conversion, the optimal Beta Compensation factor setting will be determined and applied. The BETA<2:0> bits will be automatically updated to indicate the current setting. (Default)

0 = The Beta Compensation Factor auto-detection circuitry is disabled.

bit 2-0 **BETA<2:0>:** These bits always reflect the current beta configuration settings. If auto-detection circuitry is enabled, these bits will be updated automatically, and writing to these bits will have no effect. If the auto-detection circuitry is disabled, these bits will determine the beta configuration setting that is used for the respective channels.

Care should be taken when setting the BETA<2:0> bits when the auto-detection circuitry is disabled. If the Beta Compensation factor is set at a beta value that is higher than the transistor beta, the circuit may introduce measurement errors. When measuring a discrete thermal diode (such as 2N3904) or a CPU diode that functions like a discrete thermal diode (such as an AMD processor diode), the BETA<2:0> bits should be set to '111b'.

TABLE 6-5: CPU BETA VALUES

Hex	Enable	BETA<2.0>			Minimum Beta
		2	1	0	
0h	0	0	0	0	0.11
1h	0	0	0	1	0.18
2h	0	0	1	0	0.25
3h	0	0	1	1	0.33
4h	0	1	0	0	0.43
5h	0	1	0	1	1.00
6h	0	1	1	0	2.33
7h	0	1	1	1	Disabled
8h - Fh	1	X	X	X	Auto-detection

6.13 External Diode Ideality Factor Register

REGISTER 6-10: EXTERNAL DIODE IDEALITY FACTOR REGISTER (ADDRESS 27h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	IDEALITY<5.0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
RC = Read-then-clear bit			

bit 7-6 **Unimplemented**: Read as '0'.

bit 6-0 **IDEALITY<5.0>**:This register stores the ideality factors that are applied to the external diodes. Table 6-6 defines each setting and the corresponding ideality factor. Beta Compensation and Resistance Error Correction automatically correct for most diode ideality errors; therefore, it is not recommended that these settings be updated without consulting Microchip.
For CPU substrate transistors that require the BJT transistor model, the ideality factor behaves slightly differently than for discrete diode-connected transistors. Refer to Table 6-7 when using a CPU substrate transistor.
When measuring a 65 nm Intel ® CPU, the ideality setting should be the default 12h. When measuring a 45 nm Intel CPU, the ideality setting should be 15h.

TABLE 6-6: IDEALITY FACTOR LOOK-UP TABLE (DIODE MODEL)

Setting	Factor	Setting	Factor	Setting	Factor
08h	0.9949	18h	1.0159	28h	1.0371
09h	0.9962	19h	1.0172	29h	1.0384
0Ah	0.9975	1Ah	1.0185	2Ah	1.0397
0Bh	0.9988	1Bh	1.0200	2Bh	1.0410
0Ch	1.0001	1Ch	1.0212	2Ch	1.0423
0Dh	1.0014	1Dh	1.0226	2Dh	1.0436
0Eh	1.0027	1Eh	1.0239	2Eh	1.0449
0Fh	1.0040	1Fh	1.0253	2Fh	1.0462
10h	1.0053	20h	1.0267	30h	1.0475
11h	1.0066	21h	1.0280	31h	1.0488
12h	1.0080	22h	1.0293	32h	1.0501
13h	1.0093	23h	1.0306	33h	1.0514
14h	1.0106	24h	1.0319	34h	1.0527
15h	1.0119	25h	1.0332	35h	1.0540
16h	1.0133	26h	1.0345	36h	1.0553
17h	1.0146	27h	1.0358	37h	1.0566

TABLE 6-7: SUBSTRATE DIODE IDEALITY FACTOR LOOK-UP TABLE (BJT MODEL)

Setting	Factor	Setting	Factor	Setting	Factor
08h	0.9869	18h	1.0079	28h	1.0291
09h	0.9882	19h	1.0092	29h	1.0304
0Ah	0.9895	1Ah	1.0105	2Ah	1.0317
0Bh	0.9908	1Bh	1.0120	2Bh	1.0330
0Ch	0.9921	1Ch	1.0132	2Ch	1.0343
0Dh	0.9934	1Dh	1.0146	2Dh	1.0356
0Eh	0.9947	1Eh	1.0159	2Eh	1.0369
0Fh	0.9960	1Fh	1.0173	2Fh	1.0382
10h	0.9973	20h	1.0187	30h	1.0395
11h	0.9986	21h	1.0200	31h	1.0408
12h	1.0000	22h	1.0213	32h	1.0421
13h	1.0013	23h	1.0226	33h	1.0434
14h	1.0026	d24h	1.0239	34h	1.0447
15h	1.0039	25h	1.0252	35h	1.0460
16h	1.0053	26h	1.0265	36h	1.0473
17h	1.0066	27h	1.0278	37h	1.0486

6.14 Filter Configuration Register

REGISTER 6-11: FILTER CONFIGURATION REGISTER (ADDRESS 40h)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	Filter<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'.

bit 1-0 **Filter<1:0>**: Controls the level of digital filtering that is applied to the External Diode 1 temperature measurement. See Figure 4-3 and Figure 4-4 for examples of the filter behavior.

FILTER DECODE

Filter<1:0>		Averaging
1	**0**	
0	0	Disabled (Default)
0	1	Level 1
1	0	Level 1
1	1	Level 2

6.15 Product ID Register

REGISTER 6-12: PRODUCT ID REGISTER (ADDRESS FDh)

R-0	R-1	R-1	R-0	R-0	R-0	R-0	R-0
PID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PID<7:0>:** These hard-coded bits determine the product ID.

6.16 Manufacturer ID Register

REGISTER 6-13: MANUFACTURER ID REGISTER (ADDRESS FEh)

R-0	R-1	R-0	R-1	R-1	R-1	R-0	R-1
MCHP_ID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **MCHP_ID<7:0>:** The Manufacturer ID register contains an 8-bit word that identifies Microchip as the manufacturer.

6.17 Revision Register

REGISTER 6-14: REVISION REGISTER (ADDRESS FFh)

R-0	R-0	R-0	R-0	R-0	R-1	R-1	R-0
Revision<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **REVISION<7:0>:** The Revision register contains an 8-bit word that identifies the DIE revision.

NOTES:

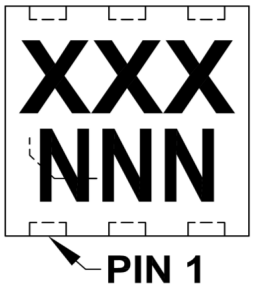
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

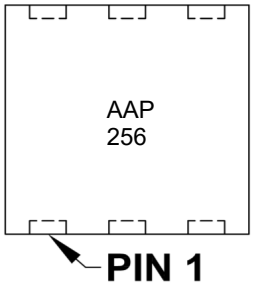
8-Lead TDFN (2x3 mm)

Example

8-Lead WDFN (2x2 mm)



Example

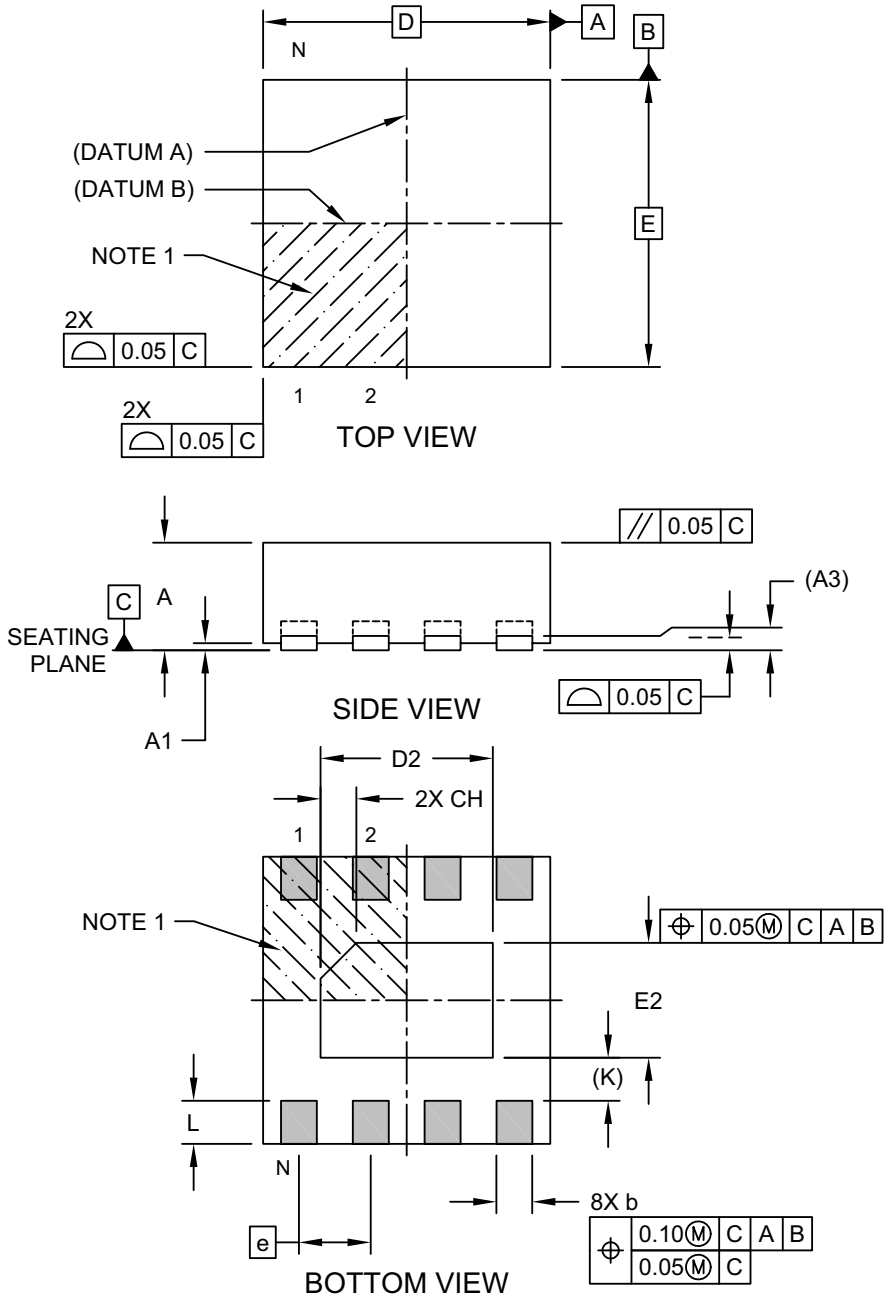


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

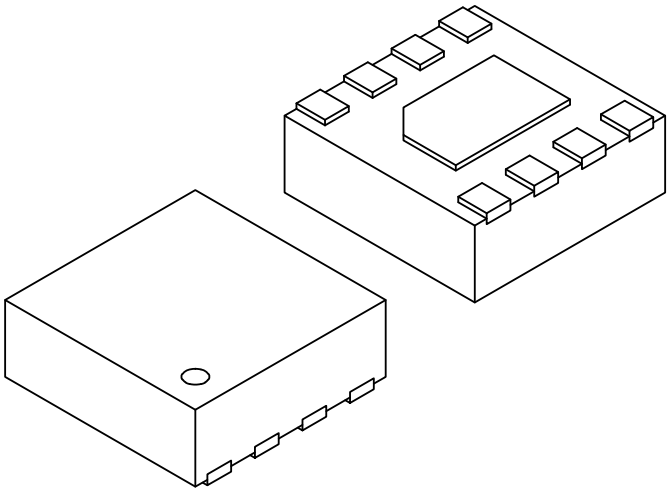


Microchip Technology Drawing C04-261C Sheet 1 of 2

a)

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.10 REF	
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.70	0.80	0.90
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.10	1.20	1.30
Exposed Pad Chamfer	CH	-	0.25	-
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.25	0.30	0.35
Terminal-to-Exposed-Pad	K		0.30 REF	

Notes:

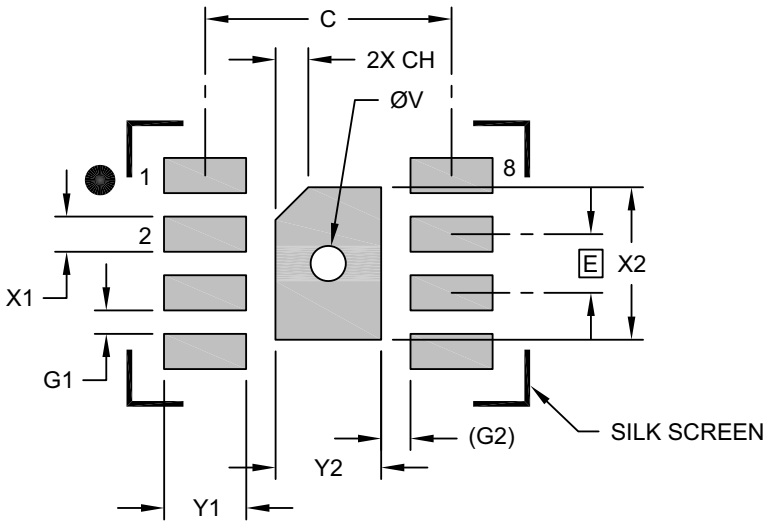
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-261C Sheet 2 of 2

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	Y2			0.90
Optional Center Pad Length	X2			1.30
Contact Pad Spacing	C		2.10	
Center Pad Chamfer	CH		0.28	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.70
Contact Pad to Contact Pad (X6)	G1	0.20		
Contact Pad to Center Pad (X8)	G2		0.25 REF	
Thermal Via Diameter	V		0.30	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

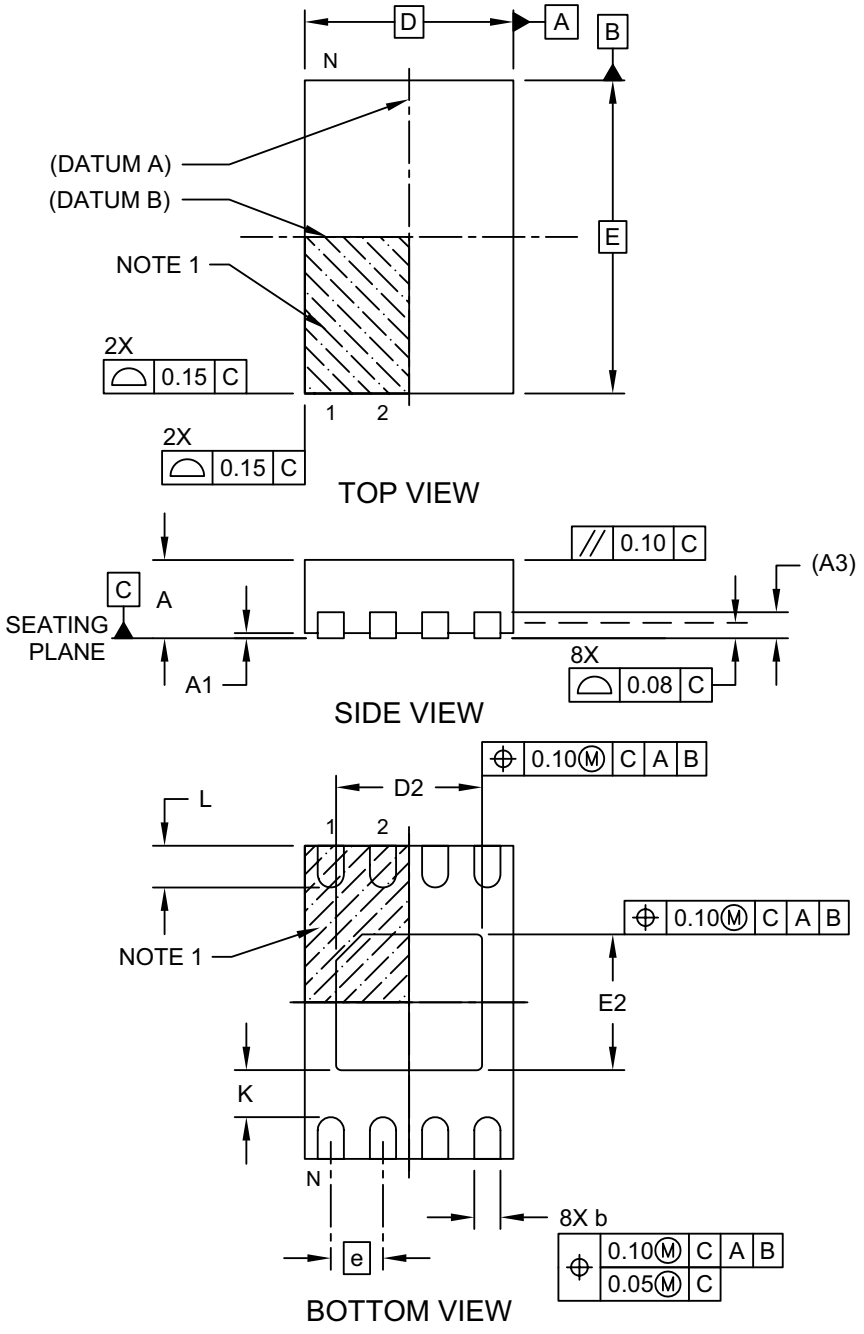
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2261C

8-Lead Plastic Dual Flat, No Lead Package (MNY) – 2x3x0.8 mm Body [TDFN]
With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

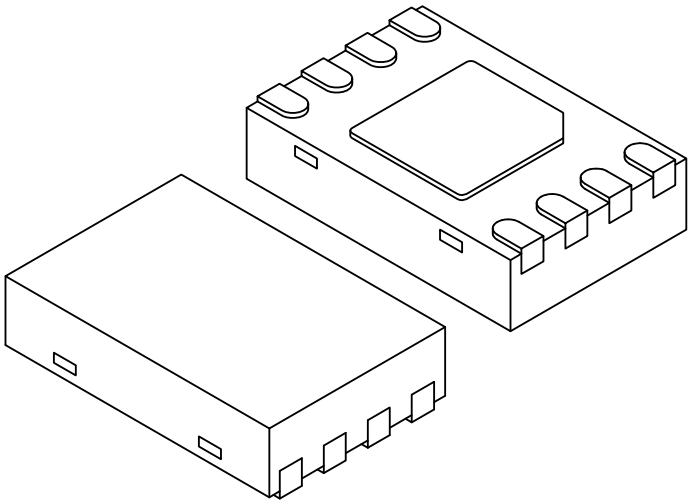
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-129-MNY Rev E Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MNY) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Exposed Pad Width	E2	1.25	1.30	1.35
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

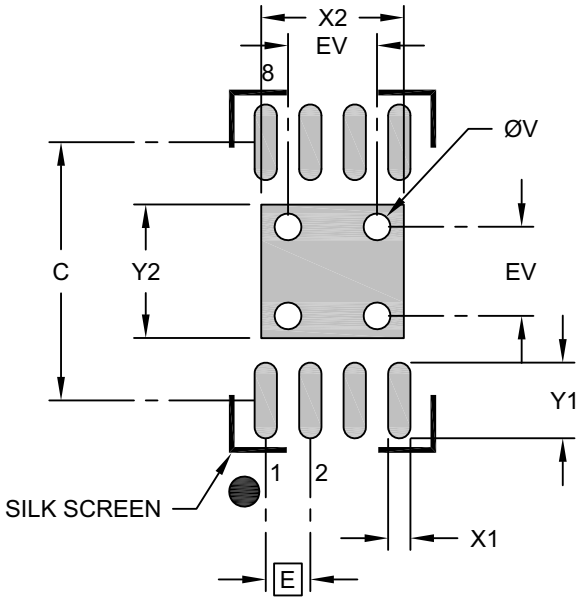
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MNY Rev E Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MNY) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.50
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.25
Contact Pad Length (X8)	Y1			0.85
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-129-MNY Rev. B

APPENDIX A: REVISION HISTORY

Revision A (July 2024)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	-XX	-X(1)
Device	I^2 Address Designator	Package	Tape and Reel

Device	EMC1462: 3.3V Multiple Channel 1°C Digital Temperature Sensor with Beta Compensation
I^2C Address Designator	A = Adjustable I^2C Address
Package Code	AC3 = Former SMSC designator for the 8-Lead, 2x3mm Body TDFN No Lead Package.
Tape and Reel	TR = Tape and Reel(1)

PART NO.	X(1)	-X	X	/XX
Device	Tape and Reel	I2C Address Designator	Temperature Range	Package Code

Device	EMC1462: 3.3V Multiple Channel 1°C Digital Temperature Sensor with Beta Compensation
Tape and Reel	T = Tape and Reel Blank = Tube
I^2C Address Designator	A = Adjustable I^2C Address
Temperature Range	E = Extended Temperature
Package Code	RW = Former SMSC designator for the 8-Lead, 2x2mm Body WDFN No Lead Package.
Tape and Reel	TR = Tape and Reel(1)

Examples:

a) EMC1462-A-AC3-TR: Adjustable I^2C Address, 8-Lead 2x3 mm TDFN Package, Tape and Reel

a) EMC1462T-AE/RW: Adjustable I^2C Address, Extended Temperature, 8-Lead 2x3 mm WDFN Package, Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Order Numbers

Ordering Number	Package	Features	Reel Quantity	SMBus Address
EMC1462-A-AC3-TR	8-Pin TDFN 2x3 mm Lead-free RoHS compliant	Two temperature sensors, ALERT and THERM pins, 125°C default Therm limit, programmable SMBus address	5,000 pcs	Selectable via ALERT pull-up
EMC1462T-AE/RW	8-Pin WDFN 2x2 mm Lead-free RoHS compliant	Two temperature sensors, ALERT and THERM pins, 125°C default Therm limit, programmable SMBus address	3,000 pcs	Selectable via ALERT pull-up

NOTES:

Note the following details of the code protection feature on Microchip products:

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