DM621

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12-CHANNELS PRE-PROGRAMMABLE

CONSTANT CURRENT LED DRIVER

新竹市科學園區展業一路 9 號 7 樓之 1
SILICON TOUCH TECHNOLOGY INC.
9-7F-1, Prosperity Road I, Science Based Industrial Park,
Hsin-Chu, Taiwan 300, R.O.C.
Tel：886-3-5645656 Fax：886-3-5645626

DM621

12-CHANNELS PRE-PROGRAMMABLE CONSTANT CURRENT LED DRIVER

General Description

The DM621 is an innovative LED driver that integrates a new data transmit interface to accomplish **2-wires** control for lighting applications. By the combination of SIN and DCK, DM621 could be pre-programmed to set the operating modes that involve GCK frequency division, PWM grayscale selection, inverse IOUT PWM signal, and GCK frequency selection. DM621 also provides the auto-latch function and incorporates a particular PWM method (AS-PWM). The IOUT waveform is averagely divided into 16 sections in order to reduce the flickers and enhance the visual refresh rate. The DM621 could also be constructed as a PWM controller for LED drivers. In this case, resistors must be connected at output pins to achieve this function (Fig.18).

This chip incorporates 4x3-channel constant current circuitry with current value set by 3 external resistors and 256/1024/4096/16384 gray scale PWM function unit. Each channel provides a maximum current of 90mA. The maximum output sustaining voltage of 28V would make more serial LEDs possible. And DM621 also integrates an internal regulator to make power supply voltage up to 12V. Meanwhile, retiming of DCKO and SOUT is advantageous in the LED decorating and long-cascade applications.

Features

- 4 x 3(R/G/B) Output Channels
- 8/10/12/14-bits PWM grayscale Control
- Maximum Clock Frequency: 20MHz
- Constant Current Output: 5mA to 90mA
- Maximum Output Sustaining voltage: 28V
- Power Supply Voltage: 5V to 12V
- Average Separated IOUT PWM Waveform
- **Auto-latch** Function
- **Retiming of DCKO and SOUT** for long cascade applications
- Serial Shift-In Architecture for Data of Grayscale, frequency Division and PWM bit number
- Incorporating internal GCK oscillator 12MHz (Refresh rate = 46.8KHz @ 8-bits PWM)
- Package: TSSOP24 (with thermal pad), QFN20 (with thermal pad)

Block Diagram

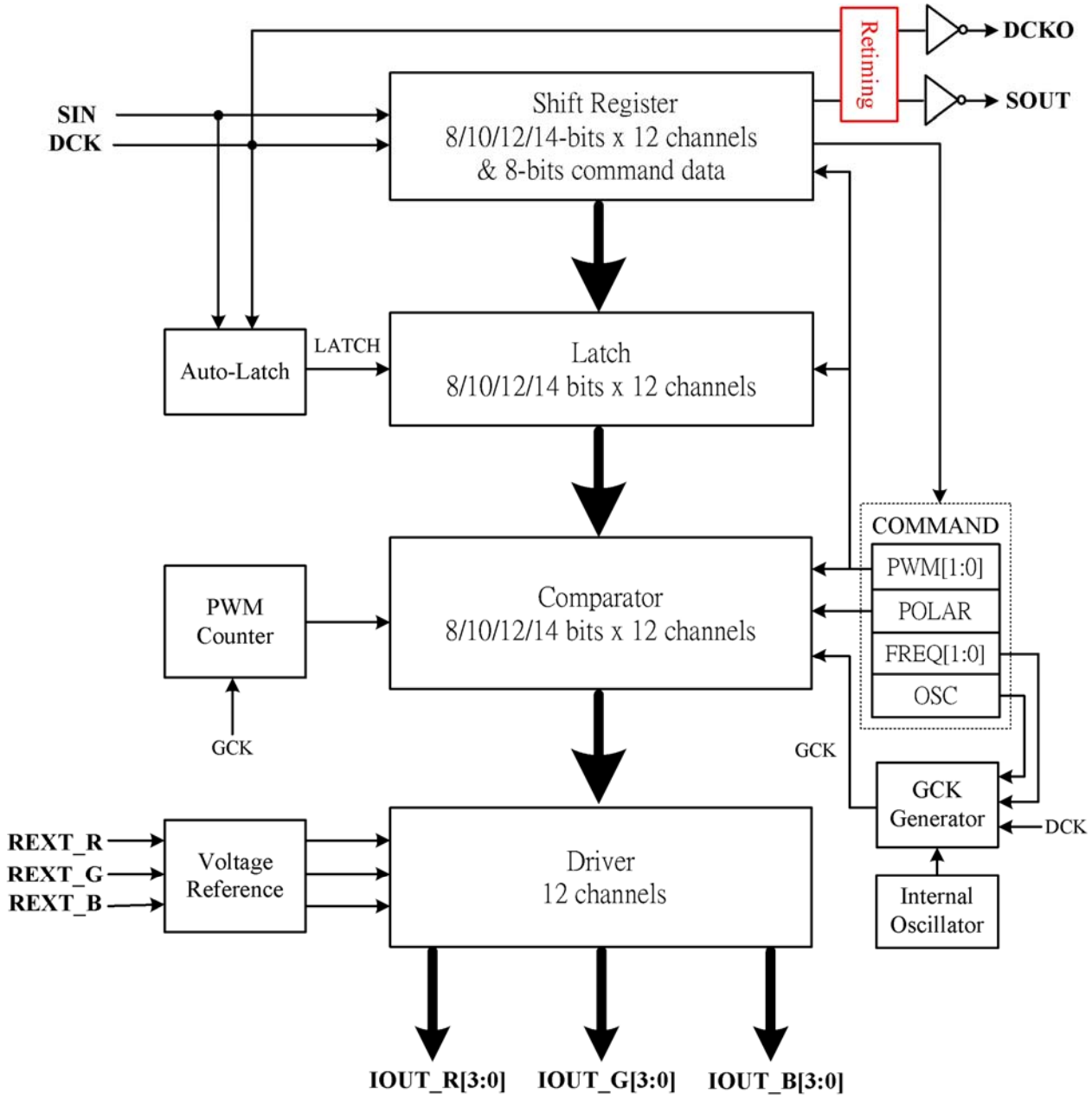


Figure 1. Functional Schematic of Whole Chip

The schematic of DM621 comprises of several fundamental units as shown in Figure1. The grayscale data and command data, transferred according to the synchronous clock DCK, are input into the SIN pin of DM621. Meanwhile, the combination of DCK and SIN data could produce the control signal to switch these two modes and achieve the auto-latch function. The **Retiming** block is advised to rearrange the timing of DCKO and SOUT in order to realize the Auto-Latch function and improve the ability of long cascade.

Pin Description

PIN NAME	FUNCTION	PIN No.
VDD	Power supply terminal	QFN20:1 ,TSSOP24:23
DCK	Synchronous clock input for serial data. The input data of SIN is transferred at rising edges of DCK. It also could be used as GCK.	QFN20:11 ,TSSOP24:11
DCKO	Synchronous clock output	QFN20:12 ,TSSOP24:12
VSS_DR	Driver ground terminal	QFN20: Thermal Pad TSSOP24:10,15,22,24
SIN	Serial input for grayscale data	QFN20:13 ,TSSOP24:13
SOUT	Serial output for grayscale data	QFN20:14 ,TSSOP24:14
REXT_R	External resistor connected between REXT and GND for driver current setting.	QFN20:2 ,TSSOP24:1
REXT_G		QFN20:3 ,TSSOP24:2
REXT_B		QFN20:4 ,TSSOP24:3
IOUT_R [3:0]	LED driver outputs	QFN20:5,8,15,18 TSSOP24:4,7,16,19
IOUT_G [3:0]		QFN20:6,9,16,19 TSSOP24:5,8,17,20
IOUT_B [3:0]		QFN20:7,10,17,20 TSSOP24:6,9,18,21

Pin Configuration (Top View)

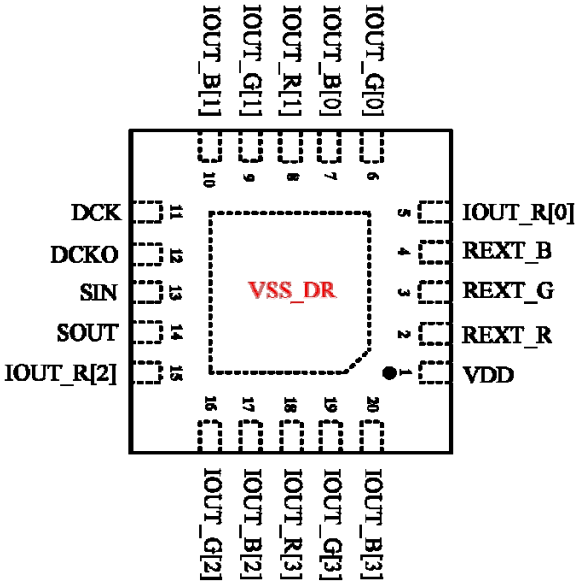


Figure 2. The Package of QFN20

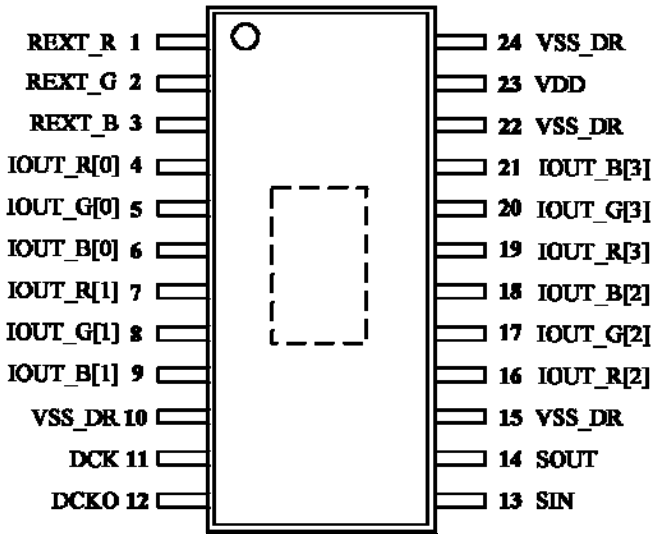
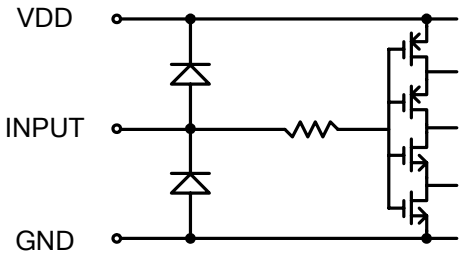


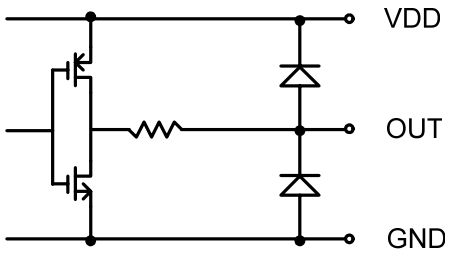
Figure 3. The Package of TSSOP24

Equivalent Circuit of Inputs and Outputs

1. DCK, SIN terminals



2. DCKO, SOUT terminals



Maximum Ratings (Ta = 25°C, $Tj_{(max)}$ = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	12	V
Input Voltage	V_{IN}	5	V
Output Current	I_{OUT}	90	mA
Output Voltage	V_{OUT}	28	V
DCK Frequency	F_{DCK}	20	MHz
IGND Terminal Current	I_{GND}	750	mA
Power Dissipation	P_D	3.1 (QFN20: Ta=25°C)	W
		2.78 (TSSOP24 exposed pad: Ta=25°C)	
Thermal Resistance	$R_{th(j-a)}$	40.21 (QFN20)	°C/W
		45 (TSSOP24 exposed pad)	
Operating Temperature	Topr	85	°C
Storage Temperature	Tstg	150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	—	5	—	12	V
Output Voltage	V_{OUT}	—	—	—	28	V
Operating Temperature	T_{OPR}	—	25	—	85	℃
Output Current	IOUT	OUT	5	—	90	mA
	I_{OH}	V_{OH} =3V	—	2.5	—	mA
	I_{OL}	V_{OL}= 0.2V	—	-2	—	mA
Input Voltage	VIH	VDD=5V~12V	3	—	5	V
	VIL		0	—	1	

Electrical Characteristics (VDD = 12 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	—		3	—	5	V
Input Voltage "L" Level	VIL	—		0	—	1	
Output Leakage Current	I_{OL}	VOUT = 28 V		—	—	1.0	uA
Output Current Skew (Bit-Bit)	∆Iout	VOUT = 1V	REXT=5 KΩ	—	—	±4	%
Output Current Skew (Chip-Chip)	∆Iout	VOUT = 1V	REXT=5 KΩ	—	—	±6	%
Output Voltage Regulation	I	Vout = 1.2V ~ 5.0V (% / Vout)	REXT=5 KΩ	—	0.1	0.5	% / V
Supply Voltage Regulation	% / VREF	VDD = 5V ~12V		—	0.5	1	% / V
Internal Oscillator Frequency	fosc	VDD = 5V ~12V		9.8	12.3	14.75	MHz
Supply Current "OFF"	Idd (off)	REXT = OPEN, all outputs off		—	1.9	—	mA
		REXT = 2KΩ (Iout=60mA), all outputs off		—	17	—	
Supply Current "ON"	Idd (on)	REXT = 2KΩ (Iout=60mA), all outputs on		—	17	—	

Switching Characteristics (Ta = 25 °C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SOUT Propagation Delay ("L" to "H")	DCK to SOUT	$t_{PLH(sout)}$	VDD=5V VIH=3V VIL=GND Rext=5KΩ VLED=5V RL=62Ω CL=8pF	10	25	40	ns
SOUT Propagation Delay ("H" to "L")		$t_{PHL(sout)}$		5	20	35	ns
DCKO Propagation Delay ("L" to "H")	DCK to DCKO	$t_{PLH(DCKO)}$		4	8	12	ns
DCKO Propagation Delay ("H" to "L")		$t_{PHL(DCKO)}$		5	10	15	ns
Output Current Rise Time		t_{or}		18	25	32	ns
Output Current Fall Time		t_{of}		8	15	22	ns
DCKO to SOUT Delay Time		t_{out}		12	—	—	ns
SIN Setup Time		t_{setup}		3	—	—	ns
SIN Hold Time		t_{hold}		8	—	—	ns
Command Delay Time		t_{CMD}		12	20	—	ns
SIN to SOUT Rise Delay Time (CMD Method)		t_{sdr}		6	9	12	ns
SIN to SOUT Fall Delay Time (CMD Method)		t_{sdf}		5	8	11	ns

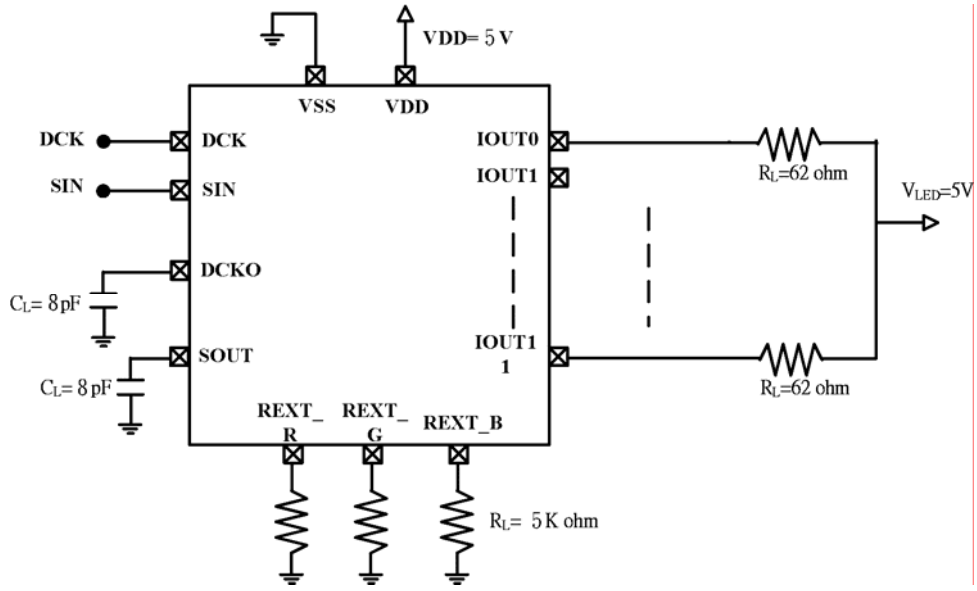


Figure 4. Measurement

Architecture

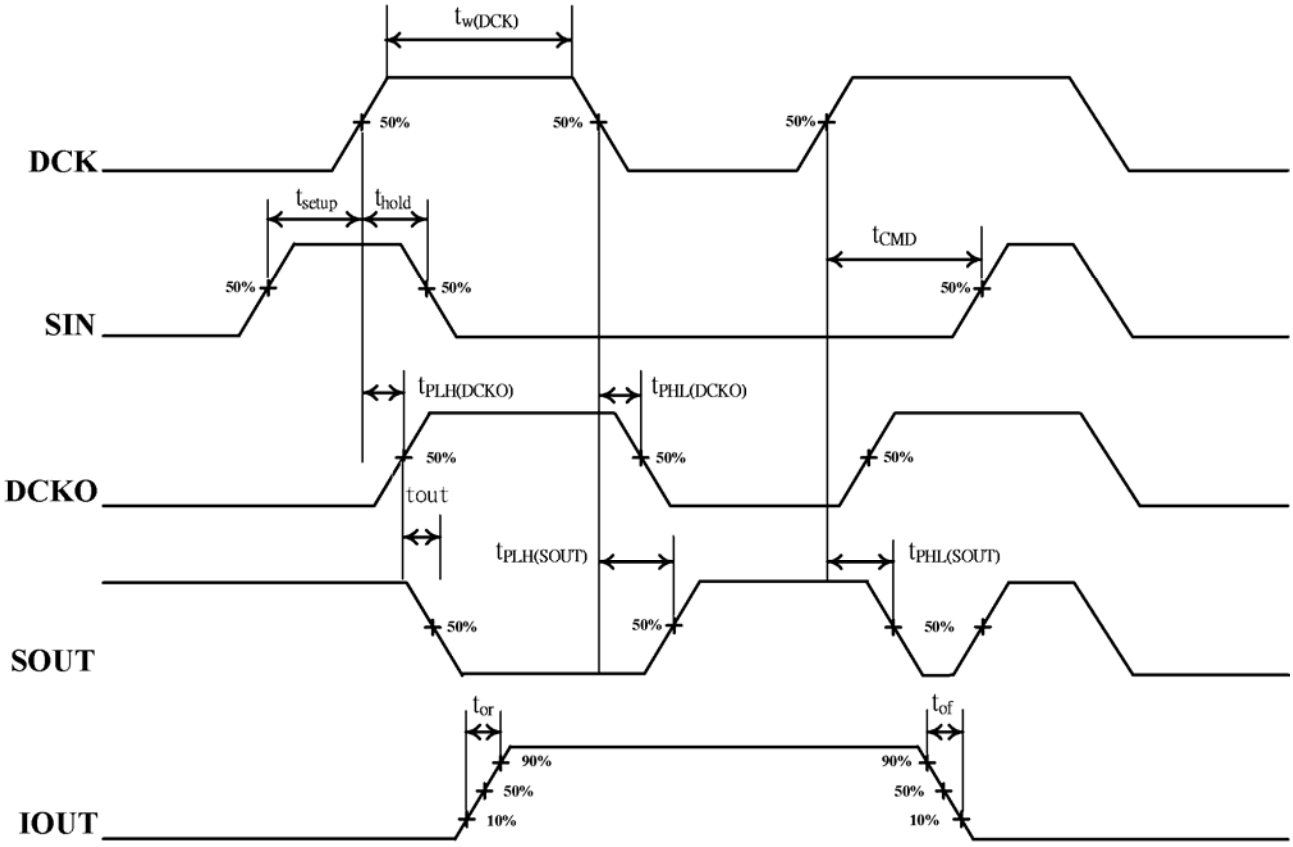
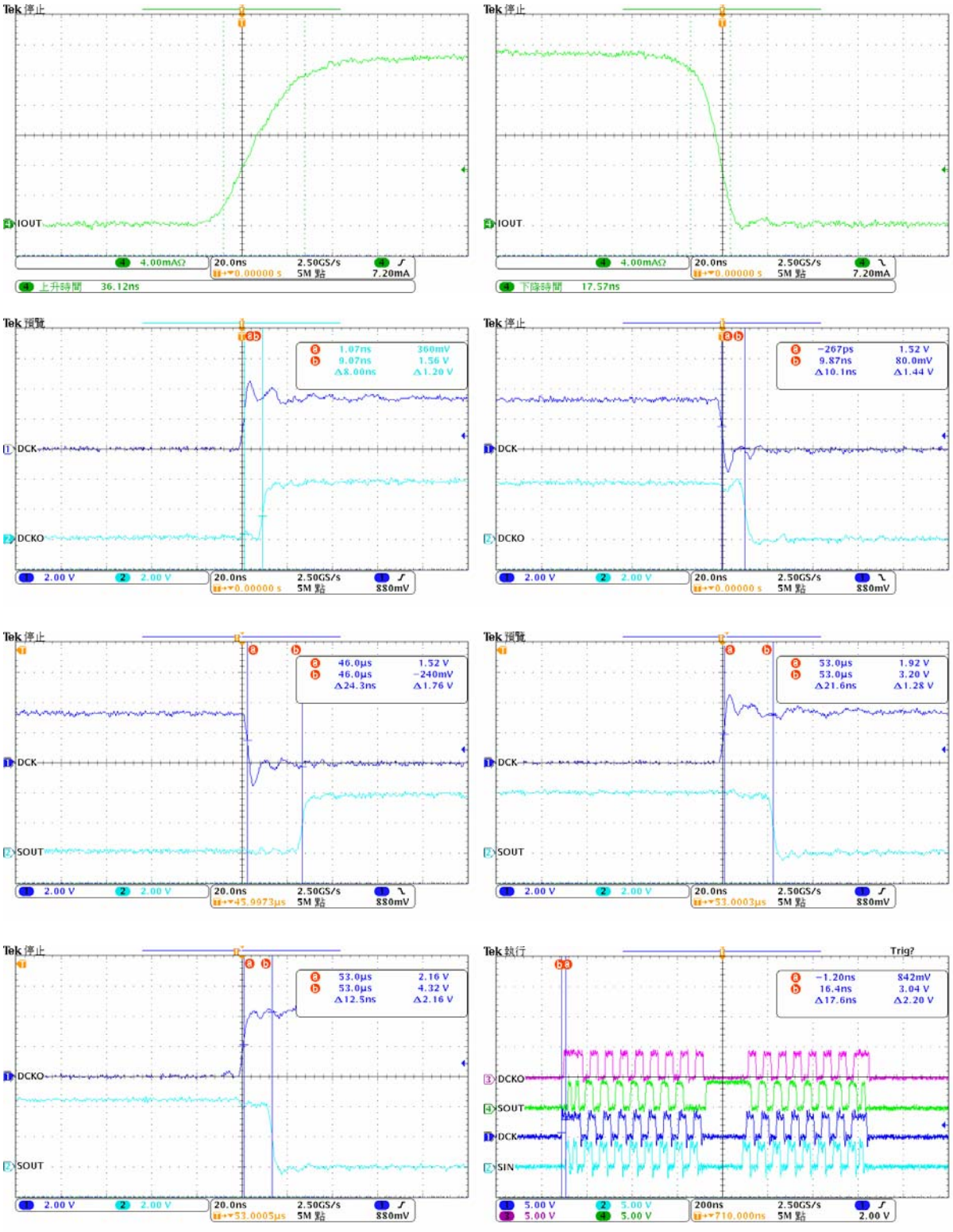


Figure 5. The Definitions of Parameters

Typical Performance Characteristics (refer to Figure.4)



Serial Shift-In Luminance Data (Shift Register Architecture)

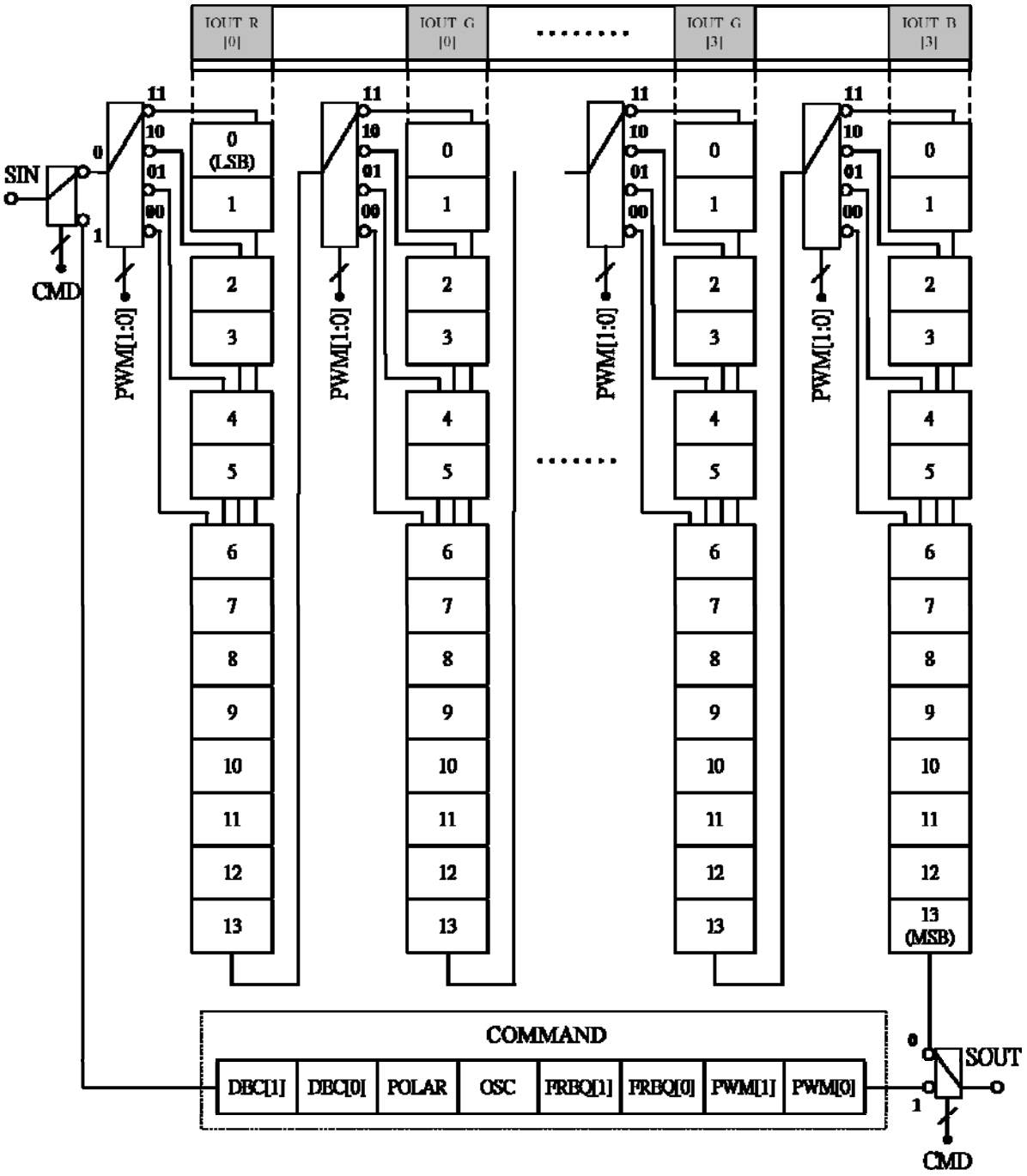


Figure 6. Serial Shift-In Luminance Data Structure

This serial shift (shift register) architecture follows a FIFO (first-in first-out) format.
The MSB (Most Significant Bit) data is the first data bit that shift into the driver.
The LSB (Least Significant Bit) data is the last bit in the data sequence.
And the PWM [1:0] command determines the data rate of each channel.

Average Separated PWM (AS-PWM) Waveform

The DM621 incorporates a new PWM method, hence the IOUT waveform demonstrates a very different characteristic compared to conventional PWM method. The IOUT waveform is averagely divided into 16 sections in a whole PWM period at each PWM mode. Furthermore, this progressive algorithm could efficiently reduce flickers and enhance the visual refresh rate.

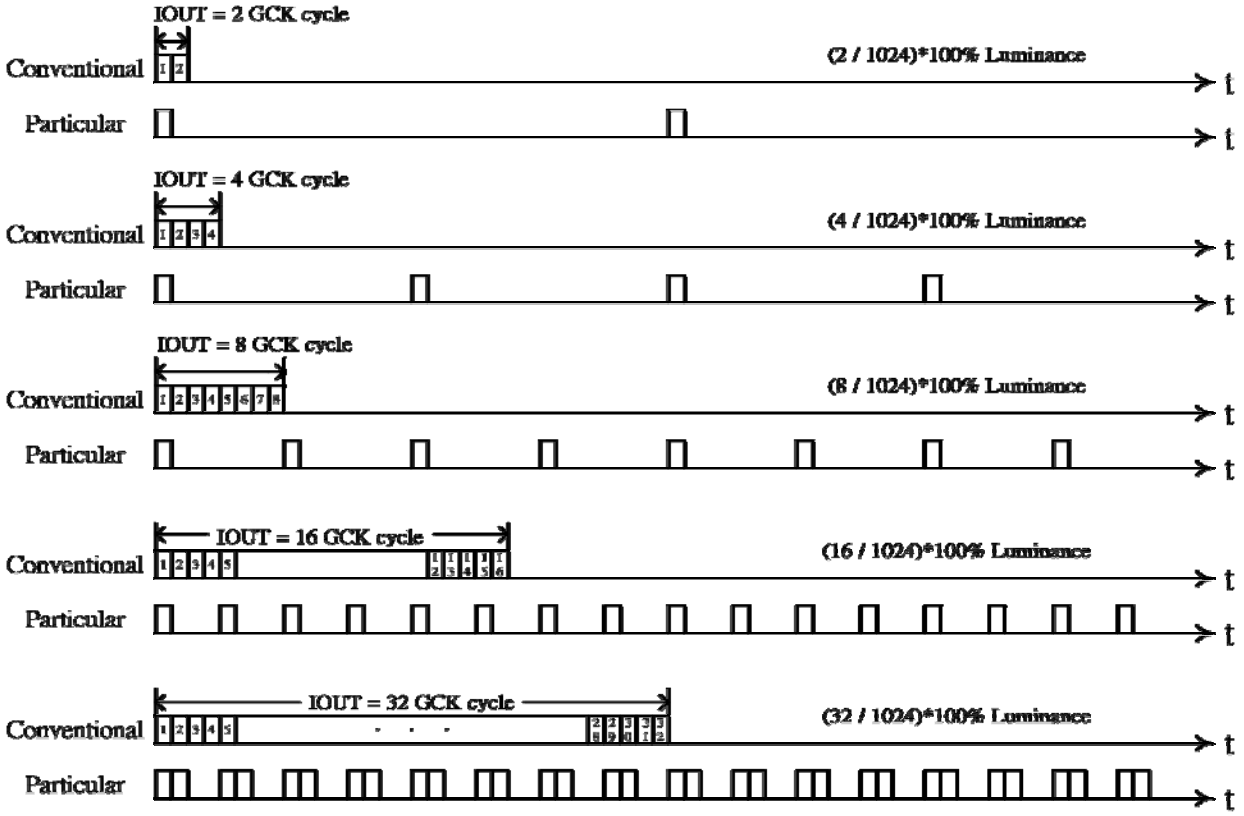


Figure 7. The Progressive PWM Method (1)

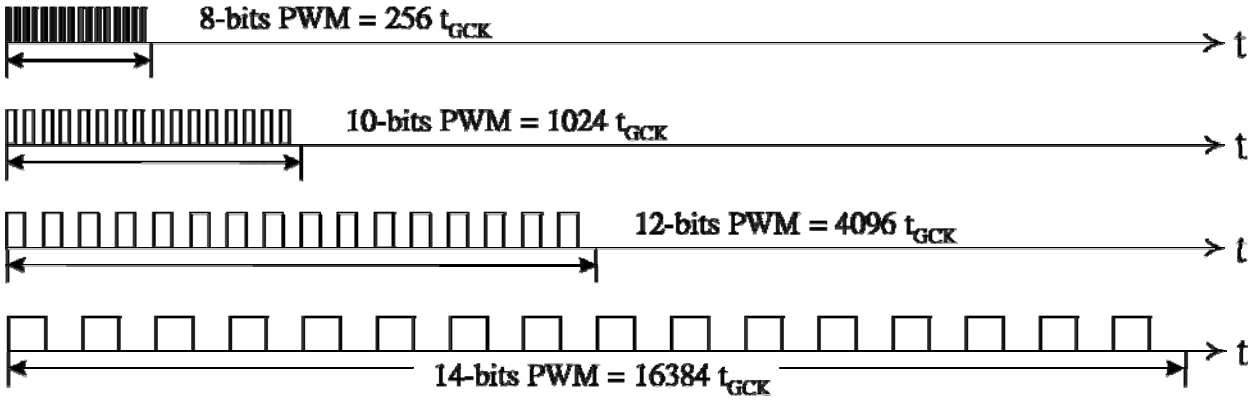


Figure 8. The Progressive PWM Method (2)

Command/Data Switching and Auto-latch Function

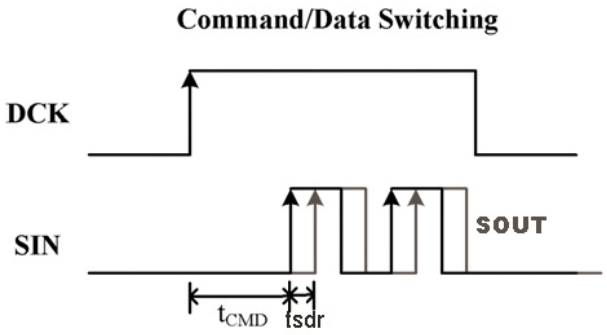


Figure 9(a). The Command/Data Method

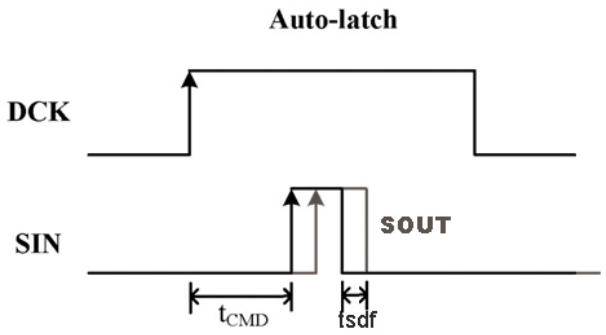


Figure 9(b). The Auto-latch Method

DM621 combines the signals of DCK and SIN to realize the Command/Data switching and Auto-latch function. When the area that DCK keeps at high level includes two positive edges of SIN, DM621 would switch automatically to the command data mode, illustrated in Figure 9(a). At this time, 8-bits command data could be transmitted to set the operating condition adequate for different applications. After command data transmission is accomplished, a latch signal would have to be executed by Auto-latch function. And this chip would latch command data into internal registers and return to the grayscale data mode as a latch instruction is executed. The Auto-latch function is realized by this method that the area that DCK keeps at high level includes only one positive edge of SIN, illustrated in Figure 9(b). Note that the latch signal of command data and grayscale data could be completed according to the same Auto-latch process.

Both Command/Data switching and Auto-latch process would produce signals to control synchronously every serial DM621s. Therefore, each serial DM621 would enter the command mode and execute a latch instruction simultaneously. And DM621 also supports the internal synchronous clock for grayscale display. These characteristics would make great grayscale display possible. In this specific design, the smallest limitation of t_{CMD}, the time from the positive edge of DCK to the first positive edge of SIN, is 20ns in order to promise the correct command and grayscale data could be received.

Note that command data have to be transmitted to pre-programmed DM621s when the system is restarted because there are no EEPROM in this chip to save the command data and the grayscale data.

Command Data

COMMAND	FUNCTION
PWM [1:0]	8/10/12/14-bits PWM mode selection PWM [1:0] = 2'b00: 8-bits PWM count PWM [1:0] = 2'b01: 10-bits PWM count PWM [1:0] = 2'b10: 12-bits PWM count PWM [1:0] = 2'b11: 14-bits PWM count
FREQ [1:0]	GCK frequency division selection FREQ [1:0] = 2'b00: GCK=CLK FREQ [1:0] = 2'b01: GCK=CLK/2 FREQ [1:0] = 2'b10: GCK=CLK/4 FREQ [1:0] = 2'b11: GCK=CLK/8
OSC	GCK source selection OSC =1'b0: Internal oscillator (12MHz) OSC =1'b1: External DCK signal
POLAR	Inverse PWM data selection POLAR =1'b0: Normal PWM signal POLAR =1'b1: Inverse PWM signal
DEC [1:0]	Command Data Error Code (avoid interference) DEC [1:0] =2'b11: Command data is enable DEC [1:0] =others: Command data is disable

Timing Diagram

By the combination of DCK and SIN data, DM621 could produce the internal CMD and LATCH signal to control the system automatically.

(*Note: CMD and LATCH are both the internal control signals)

(**Note: CMD="1" → command data mode, CMD="0" → grayscale data mode)

Command Data:

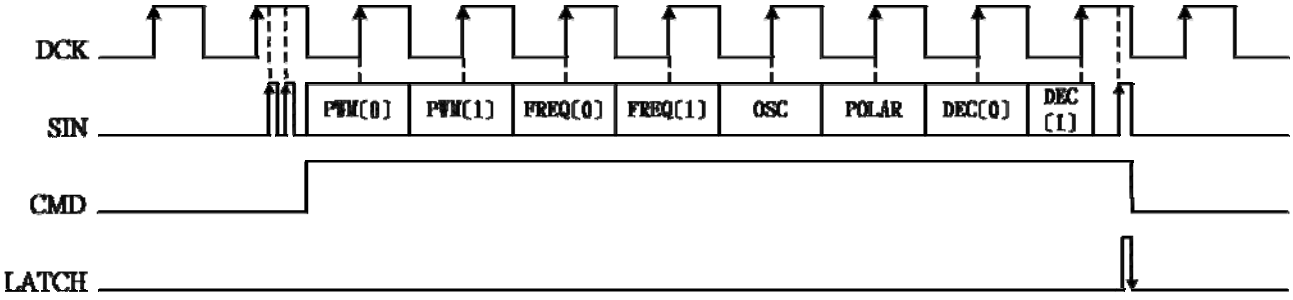


Figure 10. The timing diagram of command data

When there is two positive edges of SIN at DCK=”H”, DM621 produces CMD signal to switch to command data mode. Then users have to input 8bits command data to set the DM621 operating conditions described above. DM621 will latch command data into internal registers by incorporating one positive edge of SIN at DCK=”H”. Meanwhile, the CMD signal will return to zero.

Grayscale Data:

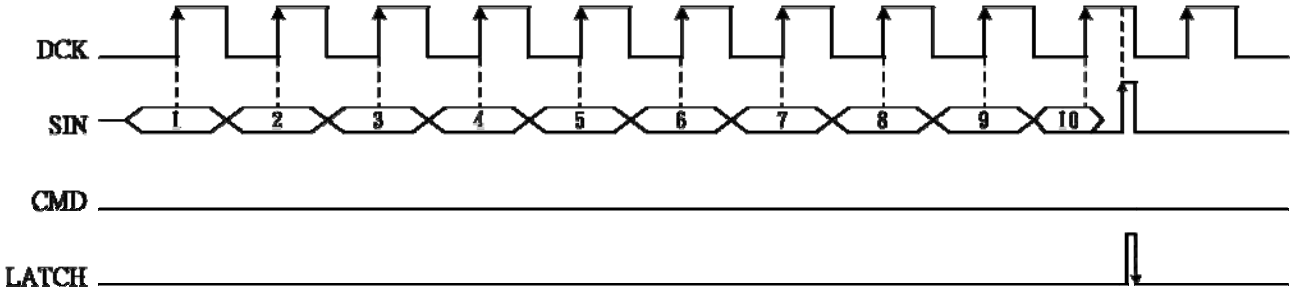


Figure 11. The timing diagram of grayscale data

According to the operating condition set at command mode, DM621 receives the 8bits/ 10bits/12bits/14bits PWM grayscale data. DM621 will latch grayscale data by incorporating one positive edges of SIN at DCK=”H”. Figure 11 is an illustration of 10-bits PWM grayscale data when the command data PWM [1:0]=2’b01.

Complete Data Transference:

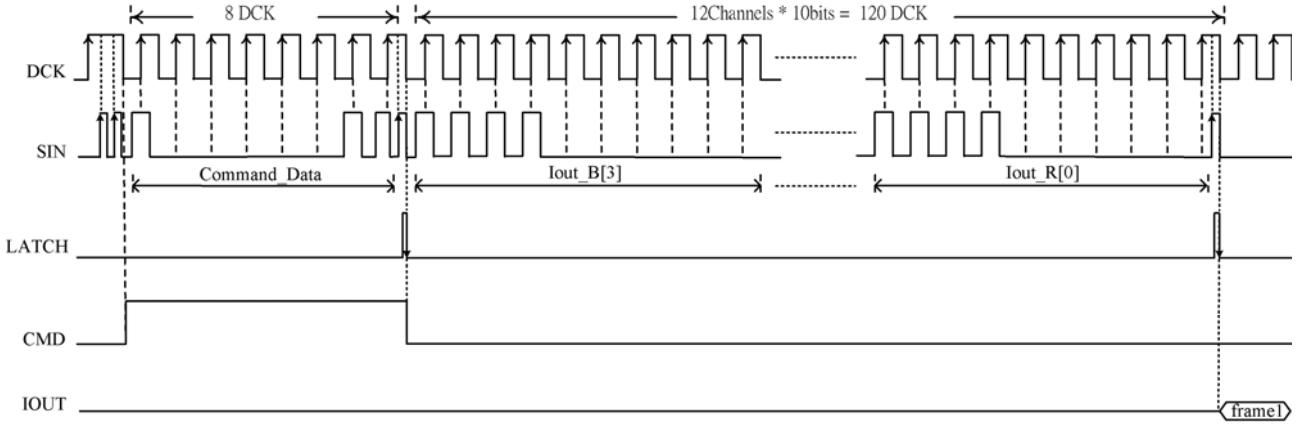


Figure 12. Detailed timing diagram of data transference

This is an illustration of the complete data transference of DM621. The command data sets the condition is 10-bits PWM mode, no GCK frequency division, no inverse PWM signal and the internal oscillator is utilized.

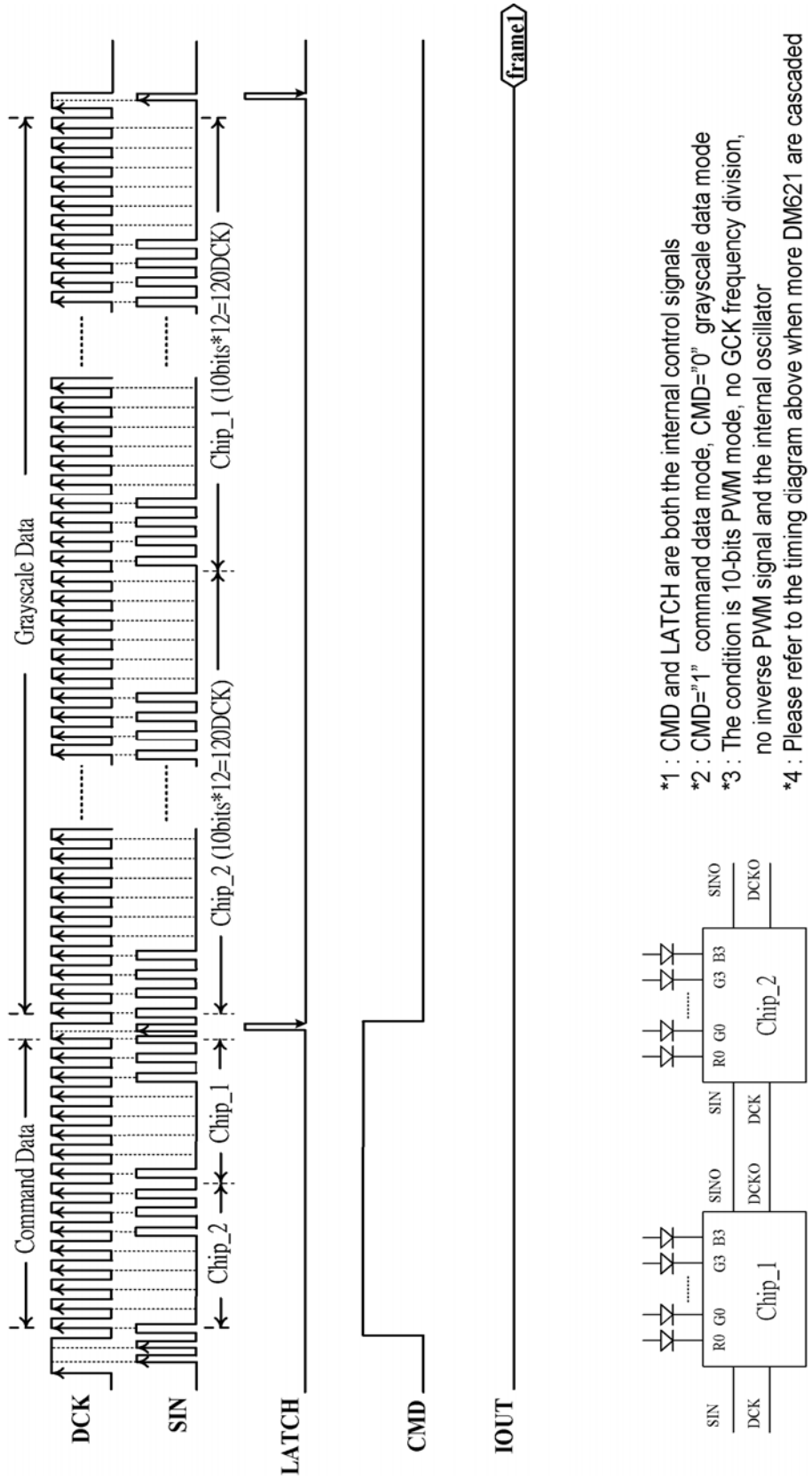


Figure 13. Timing diagram of serial data transference

Driver Output Current

Constant-current value of each output channel is set by an external resistor, which is connected between the REXT pin and GND. Varying the resistor value can adjust the current scale ranging from 5mA to 90mA. The reference voltage (Vrext) of REXT terminal is approximately 1.23V. The constant current formula is

$$IOUT(mA) = \frac{Vrext(V)}{\mathrm{Re}\,xt(k\Omega)} * 100 = \frac{1.23V}{\mathrm{Re}\,xt(k\Omega)} * 100$$

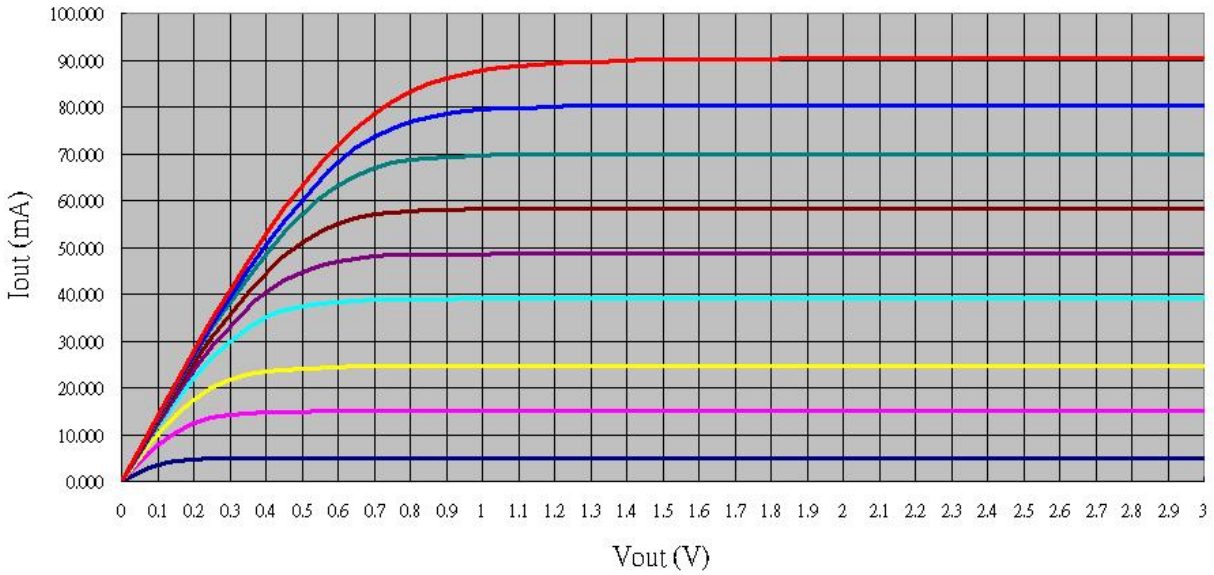


Figure 14. IOUT V.S. VOUT curve

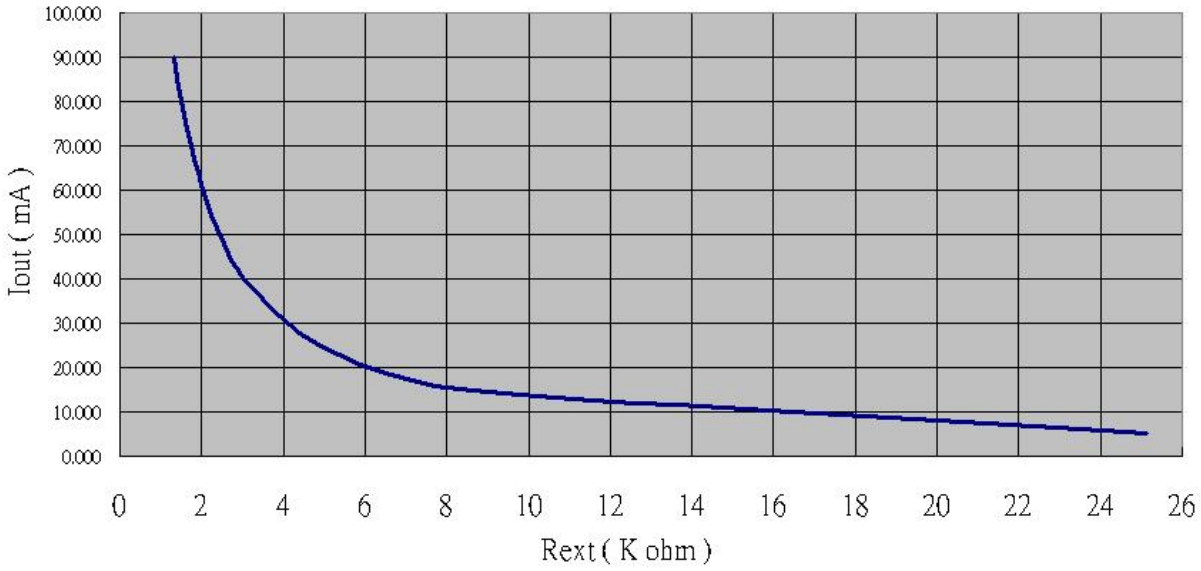


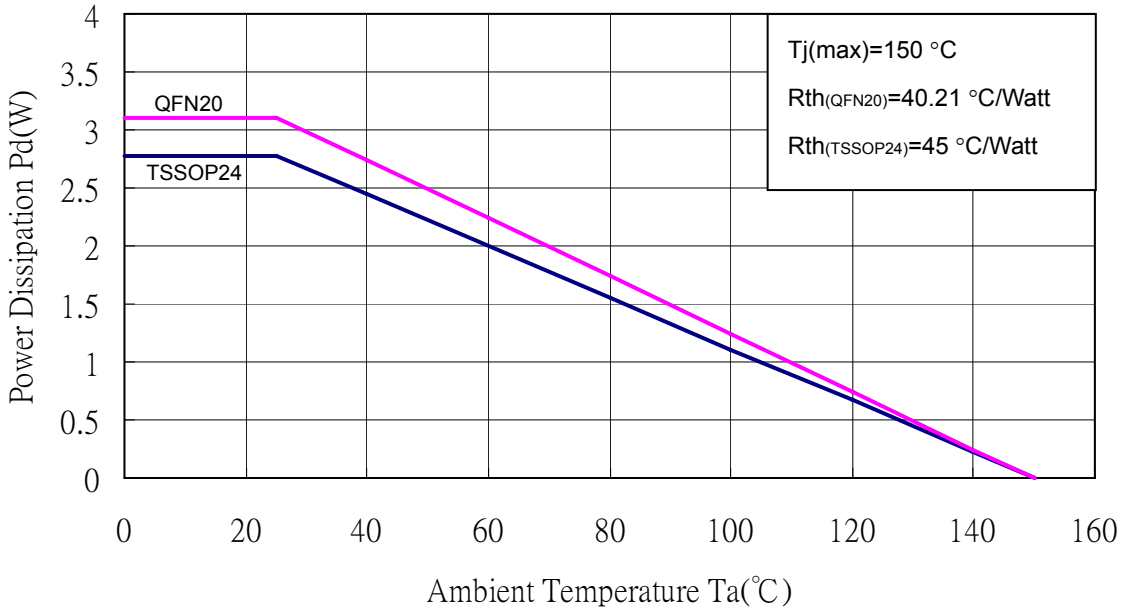
Figure 15. IOUT V.S. Rext curve

Power Dissipation

The power dissipation of a semiconductor chip is limited to its package and ambient temperature, in which the device requires the maximum output current calculated for given operating conditions. The maximum allowable power consumption can be calculated by the following equation:

$$Pd(max)(Watt) = \frac{Tj(junction\ temperature)(max)(℃) - Ta(ambient\ temperature)(℃)}{Rth(junction\text{-}to\text{-}air\ thermal\ resistance)(℃/Watt)}$$

The relationship between power dissipation and operating temperature can refer to the figure below:

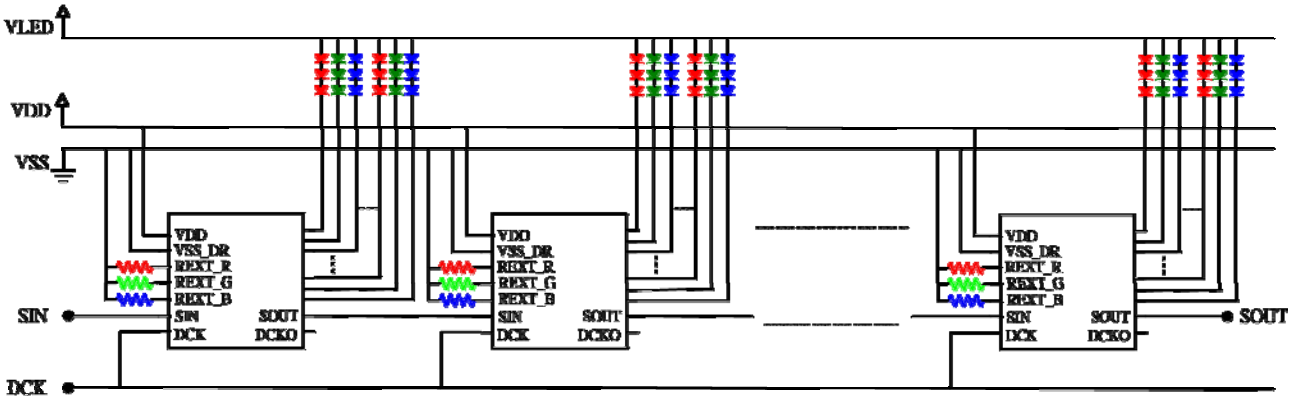


Based on the Pd (max), the maximum allowable voltage of output terminal can be determined by the following equation:

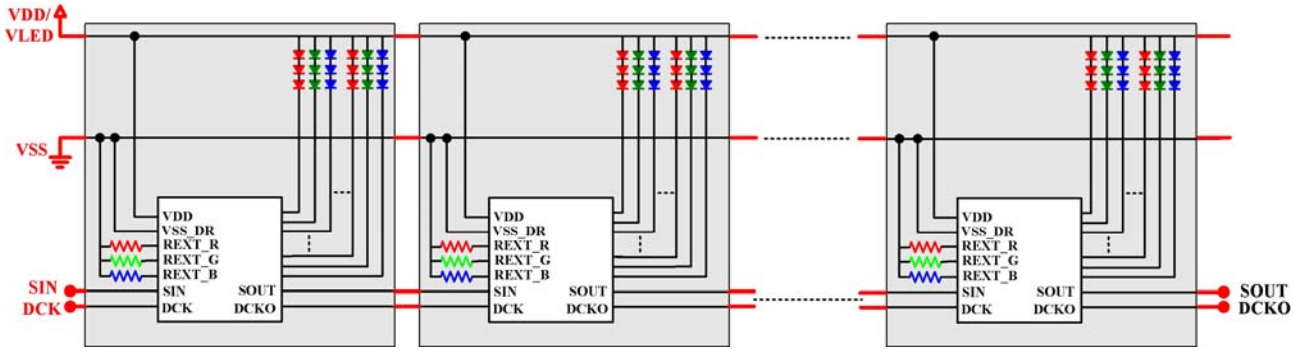
$$VoutR \times IoutR \times DutyR + VoutG \times IoutG \times DutyG + VoutB \times IoutB \times DutyB \leq Pd(max)(W) - V_{CC}(V) \times I_{DD}(A)$$

Application Diagram

(1) DCK global connection (Figure 16):

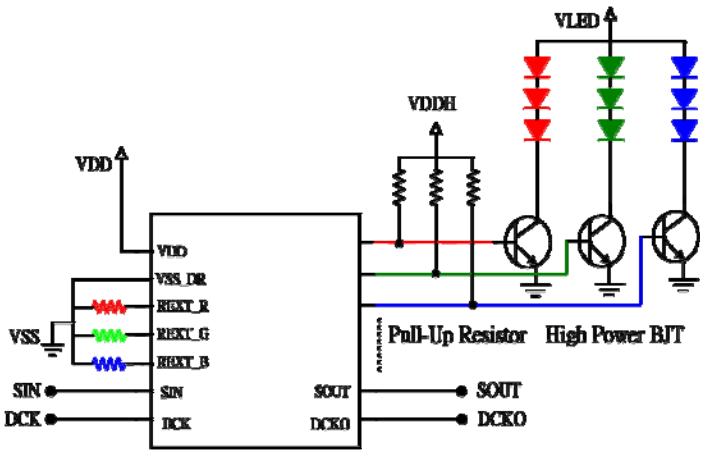


(2) DCK serial connection (Figure 17):



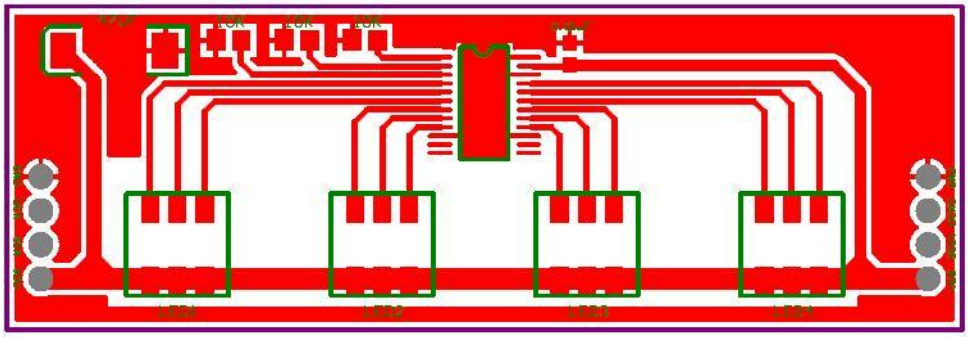
Just connected as the architecture illustrated above, DM621 could automatically produce the global latch and make serial data possible. The system just needs four lines (VDD, VSS, SIN, and DCK) to realize the cascade architecture. Please utilize a slower DCK frequency and increase t_{CMD} to realize a long cascade.

(3) PWM generator (Figure 18):

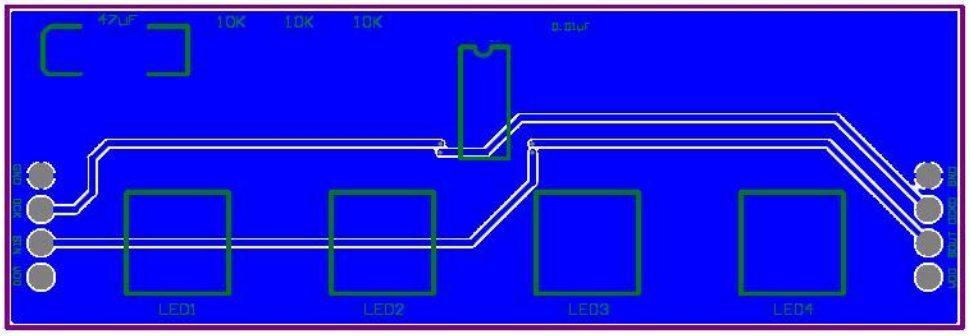


DM621 could be utilized as a PWM generator. In this case, DM621 will output inverse PWM signals by the POLAR command.

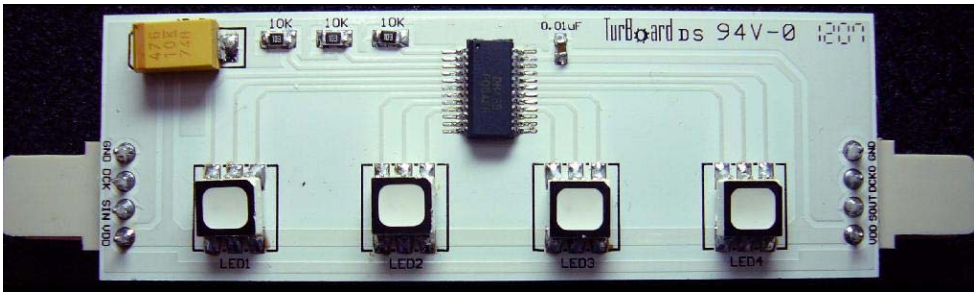
(4) Demo board (TSSOP24 PCB available):



Top View



Bottom View

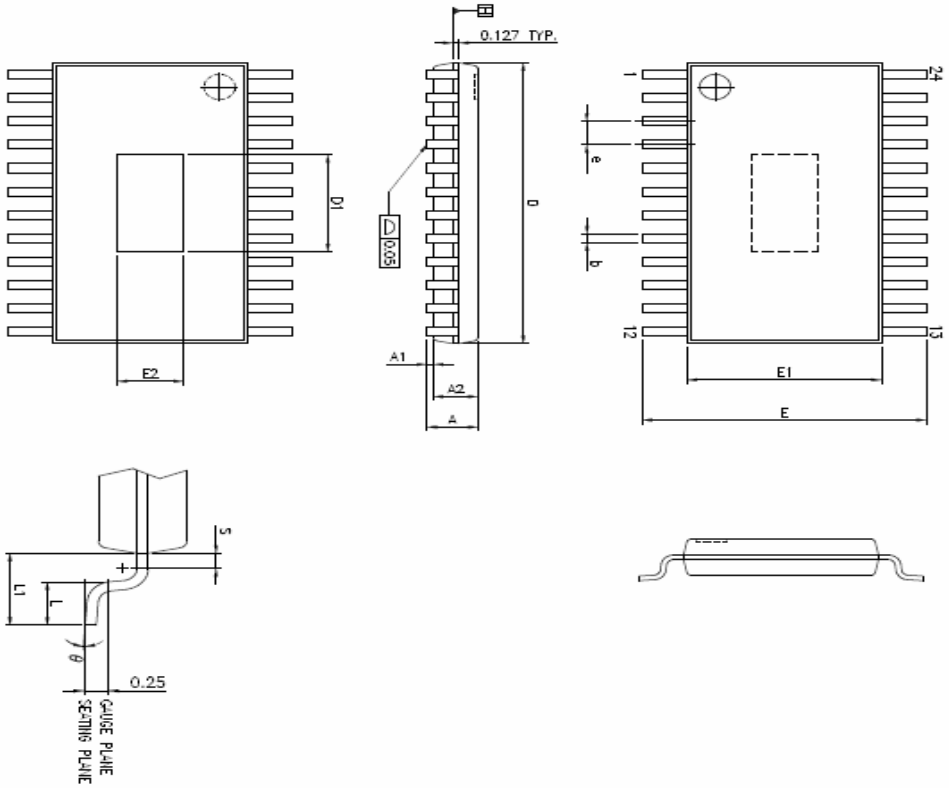


Photo

The length of DCK should be equal to that of SIN as close as possible. Similarly, DCKO and SOUT should obey this rule in order to avoid the error of timing in long-cascade applications.

Package Outline Dimension

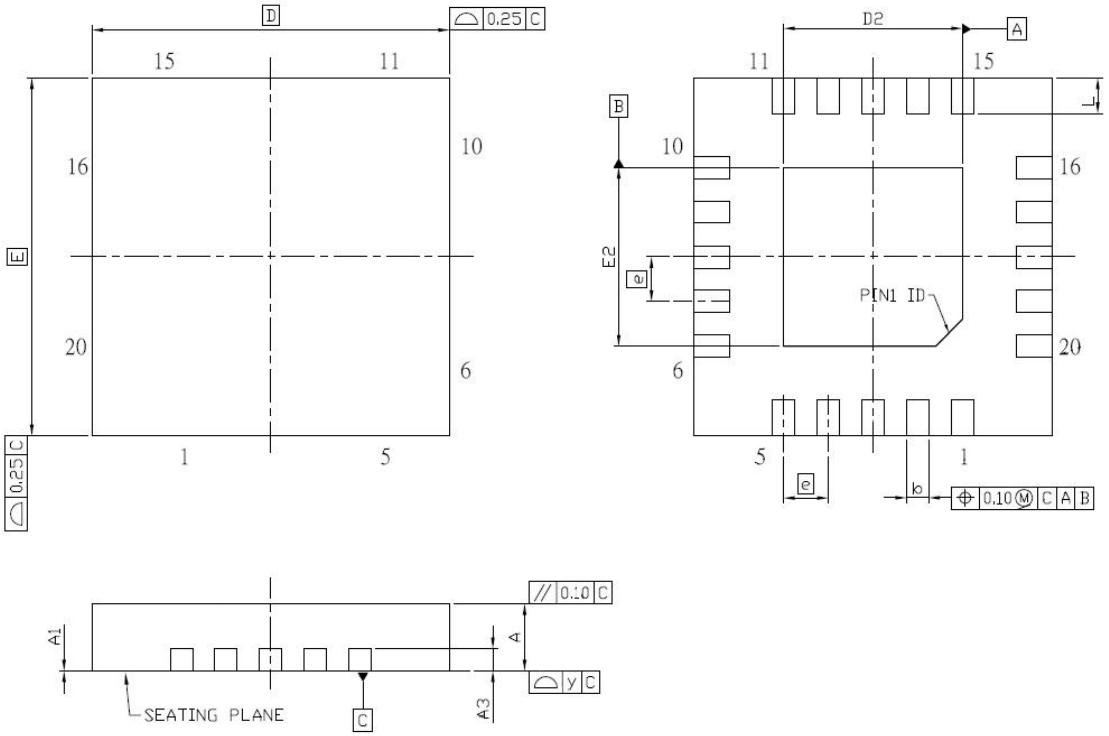
DM621-TSSOP24



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
A	-	-	1.200	-	-	0.472
A1	0.000	-	0.150	0.000	-	0.059
A2	0.800	1.000	1.050	0.315	0.394	0.413
b	0.190	-	0.300	0.074	-	0.118
D	7.700	7.800	7.900	3.031	3.071	3.110
E1	4.300	4.400	4.500	1.693	1.732	1.772
E	6.400 BSC			2.520 BSC		
e	0.650 BSC			0.256 BSC		
L1	1.000 REF			0.394 REF		
L	0.450	0.600	0.750	0.177	0.236	0.295
S	0.200	-	-	0.078	-	-
θ°	0	-	8	0	-	8
PAD SIZE2 (112×18E)						
E2	2.280	-	2.850	0.897	-	1.122
D1	3.700	-	4.620	1.456	-	1.819

Package Outline Dimension

DM621-QFN20



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
A	0.700	0.750	0.800	0.276	0.295	0.315
A1	0.000	0.020	0.050	0.000	0.020	0.020
A3	0.203 REF			0.080 REF		
b	0.180	0.250	0.300	0.071	0.098	0.118
D	3.900	4.000	4.100	1.535	1.575	1.614
D2	1.900	2.000	2.100	0.748	0.787	0.827
E	3.900	4.000	4.100	1.535	1.575	1.614
E2	1.900	2.000	2.100	0.748	0.787	0.827
e	0.500 BSC			0.197 BSC		
L	0.300	0.400	0.500	0.118	0.157	0.197
y	-	-	0.080	-	-	0.031

The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.

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