DM13H

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16-Channel Constant Current LED Driver with Error Detection

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DM13H

16-Channel Constant Current LED Driver With Error Detection

General Description

DM13H is a 16-channel constant-current sink driver specifically designed for LED display applications. The device incorporates shift registers, data latches, and constant current circuitry on the silicon CMOS chip. The maximum output current of each channel is set by a single external resistor. Overall output currents can be adjusted by a 7-bit serial shift-in data. Its built-in LED open/short detection, output channels short to GND detection help users to detect LED failures, outputs short. The thermal alarm and shutdown functions provide the over-temperature protection.

Features

- 16-Channel Constant-current outputs: 3mA to 90mA adjustable by one external resistor
- Maximum output voltage: 17V
- Maximum cascade clock frequency: 25MHz
- 7-bit linear global brightness control
- Built-in LED open/short detection: Real-time detection or Smart detection
- Built-in Outputs short to GND detection: Real-time or Smart detection
- Fast detecting response: 100ns (min.)
- Over temperature protection: Alarm (junction temperature > 130°C)
  Shutdown (junction temperature > 170°C)
- Sleep mode (sleep current : 5uA)
- In-rush current control
- Schmitt trigger input
- Power supply voltage: 3.0V to 5.5V
- Package pin assignment compatible to conventional LED drivers (DM134B/5B,DM13C)

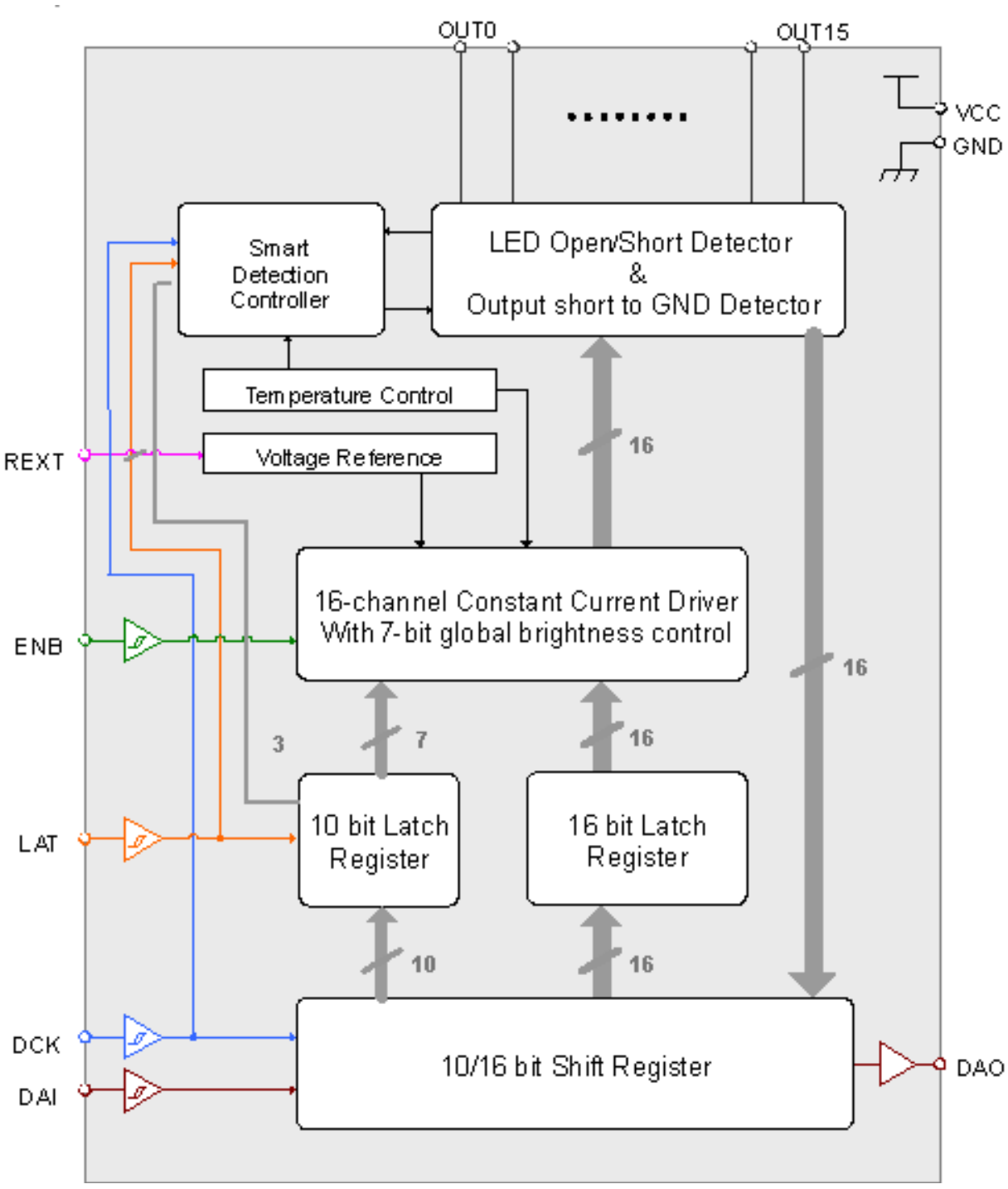
Applications

- LED Variable Message Signs (VMS) System
- Indoor/Outdoor LED Video Display

Packages

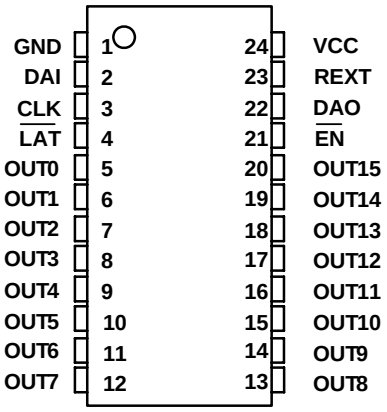
SOP24, SSOP24, TSSOP24E, SOP24B, QFN24

Block Diagram

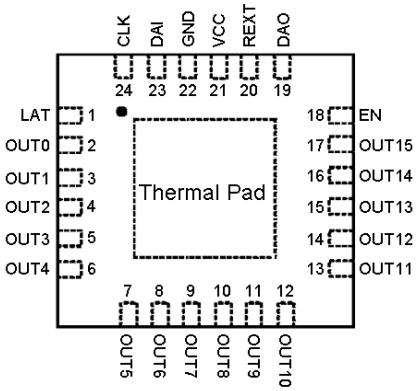


Pin Connection (Top View)

SOP24 / SSOP24 / TSSOP24E / SOP24B



QFN24

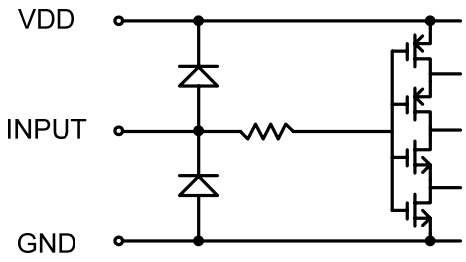


Pin Description

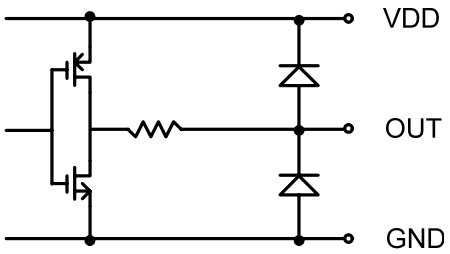
PIN No.	PIN NAME	FUNCTION
SOP24 / SSOP24 / TSSOP24E / SOP24B: 1 QFN24: 22	GND	Ground terminal.
SOP24 / SSOP24 / TSSOP24E / SOP24B: 2 QFN24: 23	DAI	Serial data input terminal.
SOP24 / SSOP24 / TSSOP24E / SOP24B: 3 QFN24: 24	CLK	Synchronous clock input terminal for serial data transfer. Data is sampled at the rising edge of CLK.
SOP24 / SSOP24 / TSSOP24E / SOP24B: 4 QFN24: 1	$\overline{LAT}$	Input terminal of data strobe. Data on shift register goes through at the rising edge (edge trigger). Otherwise, data is latched.
SOP24 / SSOP24 / TSSOP24E / SOP24B: 5~20 QFN24: 2~17	OUT0~15	Sink constant-current outputs (open-drain).
SOP24 / SSOP24 / TSSOP24E / SOP24B: 21 QFN24: 18	$\overline{EN}$	Output enable terminal: '**H**' for all outputs are turned off , '**L**' for all outputs are active.
SOP24 / SSOP24 / TSSOP24E / SOP24B: 22 QFN24: 19	DAO	Serial data output terminal.
SOP24 / SSOP24 / TSSOP24E / SOP24B: 23 QFN24: 20	REXT	External resistors connected between REXT and GND for output current value setting.
SOP24 / SSOP24 / TSSOP24E / SOP24B: 24 QFN24: 21	VCC	Supply voltage terminal.

Equivalent Circuit of Inputs and Outputs

1.CLK, DAI, $\overline{LAT}$, $\overline{EN}$ terminals (Schmitt Trigger Input)



2. DAO terminals



Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VCC	-0.3 ~ 7.0	V
Input Voltage	VIN	-0.3 ~ VCC+0.3	V
Output Current	IOUT	90	mA
Output Voltage	VOUT	-0.3 ~ 17	V
Input Clock Frequency	FCKI	30	MHz
GND Terminal Current	IGND	1500	mA
Power Dissipation	PD	1.5 (SSOP24)	W
		2.8 (TSSOP24)	
Thermal Resistance	Rth(j-a)	85 (SSOP24)	°C/W
		45 (TSSOP24E)	
Operating Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VCC	—	3.0	—	5.5	V
Output Voltage	VOUT	Driver Off *1	—	—	17	V
Output Current	IO	OUTn, VCC=5V	3	—	90	mA
	IOH	VOH = VCC – 0.2 V	—	—	+1.5	
	IOL	VOL = 0.2 V	—	—	-1.5	
Input Voltage	VIH	VCC = 3.3 V ~ 5V	0.7VCC	—	VCC	V
	VIL		0.0	—	0.3VCC	
Input Clock Frequency	FCKI	Single Chip Operation	—	—	30	MHz
		Cascade Operation			—	
$\overline{LAT}$ Pulse Width	tw$\overline{LAT}$	VCC = 5.0V	15	—	—	ns
CLK Pulse Width	tw CLK		13	—	—	
$\overline{EN}$ Pulse Width	tw$\overline{EN}$		50	—	—	
Set-up Time for DAI	tsetup(D)		10	—	—	
Hold Time for DAI	thold(D)		10	—	—	
Set-up Time for $\overline{LAT}$	tsetup(L)		10	—	—	
Hold Time for $\overline{LAT}$	thold(L)		10	—	—	
$\overline{LAT}$ Pulse Width	tw$\overline{LAT}$	VCC =3.3V	15	—	—	ns
CLK Pulse Width	tw CLK		13	—	—	
$\overline{EN}$ Pulse Width	tw$\overline{EN}$		50	—	—	
Set-up Time for DAI	tsetup(D)		12	—	—	
Hold Time for DAI	thold(D)		8	—	—	
Set-up Time for $\overline{LAT}$	tsetup(L)		8	—	—	
Hold Time for $\overline{LAT}$	thold(L)		12	—	—	

*1 The driver output voltage including any overshoot stress has to be compliant with the maximum voltage (17V).

Electrical Characteristics (VCC = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VCC	—	VCC	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VCC	
Output Leakage Current	IOL	VOH = 17 V	—	—	+1	uA
Output Voltage (S-OUT)	VOL	IOL = -1.5 mA	—	—	0.2	V
	VOH	IOH= 1.5 mA	VCC-0.2	—	—	
Output Current Skew (Channel-to-Channel) *1	IOL1	VOUT = 1.0 V Rrext = 3.9 KΩ	—	—	±4	%
Output Current Skew (Chip-to-Chip) *2	IOL2		—	—	±6	%
Output Voltage Regulation	% / VOUT	Rrext = 3.9 KΩ VOUT = 1 V ~ 3 V	—	±0.1	±0.5	% / V
Supply Voltage Regulation	% / VCC	Rrext = 3.9 KΩ	—	±1	±4	
Differential Linearity	DNL	Rrext = 3.9 KΩ	—	±1.2		LSB
Output Voltage Short to GND, LED Open Detection Threshold	V(od)	output turns on	—	0.1	—	V
LED Short Detection Threshold *3 (output turns on)	V(sd)	SV = "H"	—	VCC	—	V
		SV = "L"	—	5/6VCC	—	V
Thermal Threshold	T(130)	junction temperature	—	130	—	°C
	T(170)		—	170	—	
Thermal Shutdown Threshold	T(sht)		—	170	—	
Supply Current (Input signal is static)	$I_{DD(off)}$	power on all pins are open unless VCC and GND	—	1.2	—	mA
	$I_{DD(off)}$	Rrext = 3.9 KΩ all outputs turn off	—	7		
	$I_{DD(on)}$	Rrext = 3.9 KΩ all outputs turn on	—	7.6	—	
	$I_{DD(off)}$	Rrext = 820 Ω all outputs turn off	—	27.5		
	$I_{DD(on)}$	Rrext = 820 Ω all outputs turn on	—	30	—	
	$I_{DD(sleep)}$	Sleep current	—	5		uA

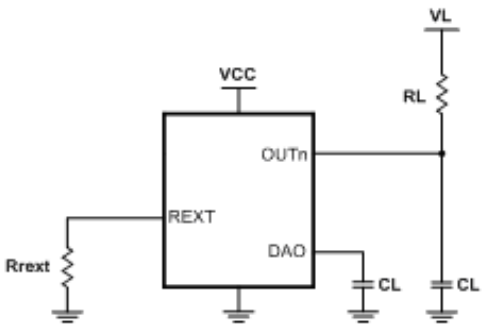
*1 Channel-to-channel skew is defined as the ratio between (any Iout – average Iout) and average Iout, where average Iout = (Imax + Imin) / 2.
*2 Chip-to-Chip skew is defined as the range into which any output current of any IC falls.
*3 LED short detection voltage level default value is VCC , refer to Page 12 for level selection.

Switching Characteristics (VCC = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L to 'H')	$\overline{EN}$ -to-OUT0	tpLH	VIH = VCC VIL = GND Rrext = 3.9 KΩ VL = 5.0 V RL = 0.18 KΩ CL = 13 pF	14	26	36	ns
	$\overline{LAT}$ -to-OUT0			19	31	41	
	CLK-to-DAO			15	19	23	
Propagation Delay ('H' to 'L')	$\overline{EN}$ -to-OUT0	tpHL		19	31	41	
	$\overline{LAT}$ -to-OUT0			19	32	41	
	CLK-to-DAO			16	20	24	
Output Current Rise Time		tor		4.5	10	18	
Output Current Fall Time		tof		4.5	10	18	
Output Delay Time ($OUT_{(n)}$-to-$OUT_{(n+1)}$)		tod		0.5	3	5.5	
Detection Response		tdet		20	100	120	

Switching Characteristics (VCC = 3.3V, Ta = 25°C unless otherwise noted)

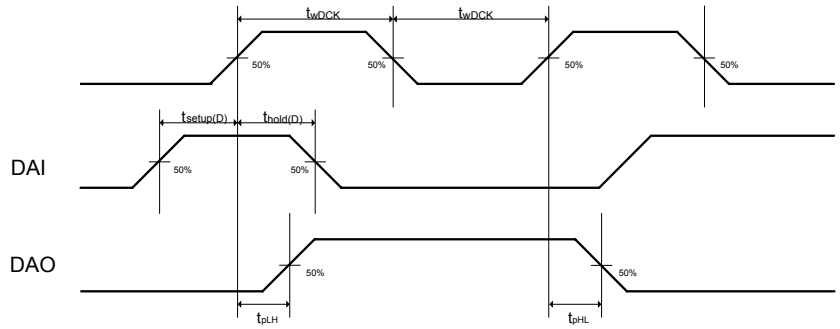
CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L to 'H')	$\overline{EN}$ -to-OUT0	tpLH	VIH = VCC VIL = GND Rrext = 3.9 KΩ VL = 5 V RL = 0.18 KΩ CL = 13 pF	16	36	46	ns
	$\overline{LAT}$ -to-OUT0			21	37	47	
	CLK-to-DAO			18	22	26	
Propagation Delay ('H' to 'L')	$\overline{EN}$ -to-OUT0	tpHL		19	35	41	
	$\overline{LAT}$ -to-OUT0			19	37	41	
	CLK-to-DAO			19	23	27	
Output Current Rise Time		tor		7.5	14	21	
Output Current Fall Time		tof		7.5	14	21	
Output Delay Time ($OUT_{(n)}$-to-$OUT_{(n+1)}$)		tod		0.7	3	6.5	
Detection Response		tdet		20	100	120	



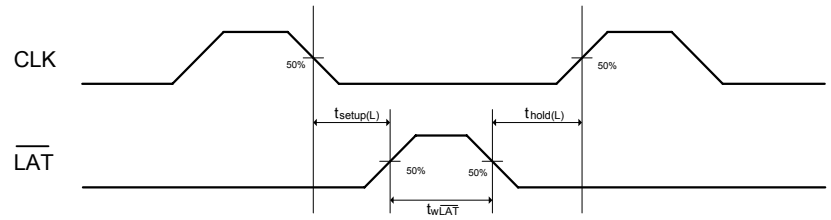
Switching Characteristics Test Circuit

Timing Diagram

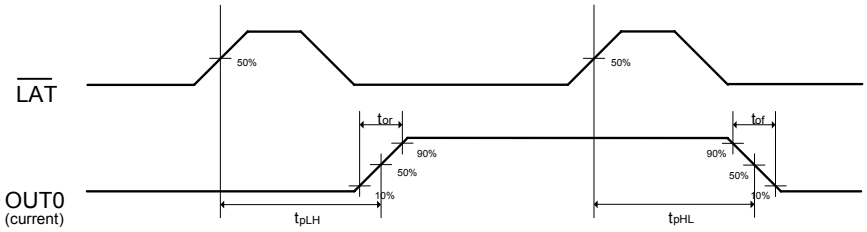
1. CLK-DAI, DAO



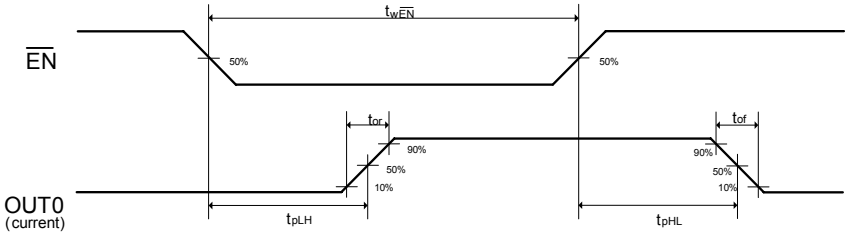
2. CLK-$\overline{LAT}$



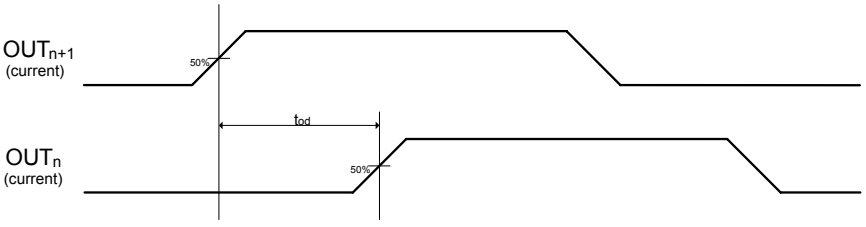
3. $\overline{LAT}$ -OUT0



4. $\overline{EN}$-OUT0

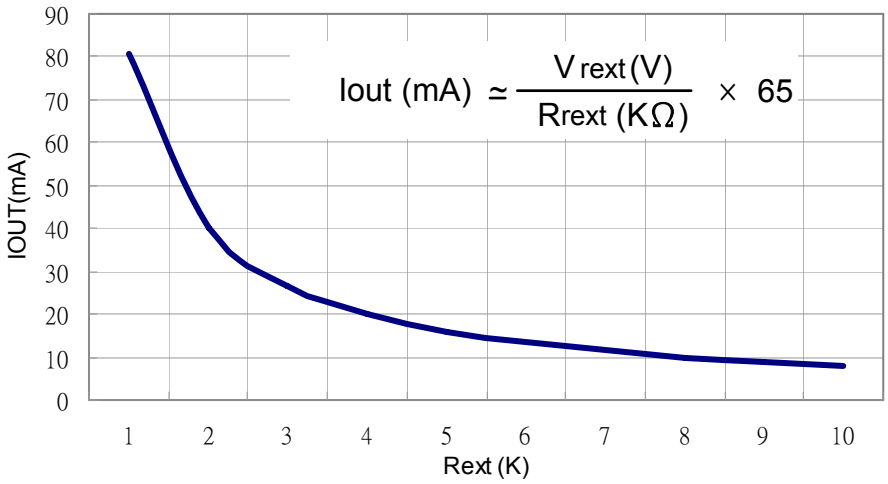


5. OUT_{n+1}-OUT_n

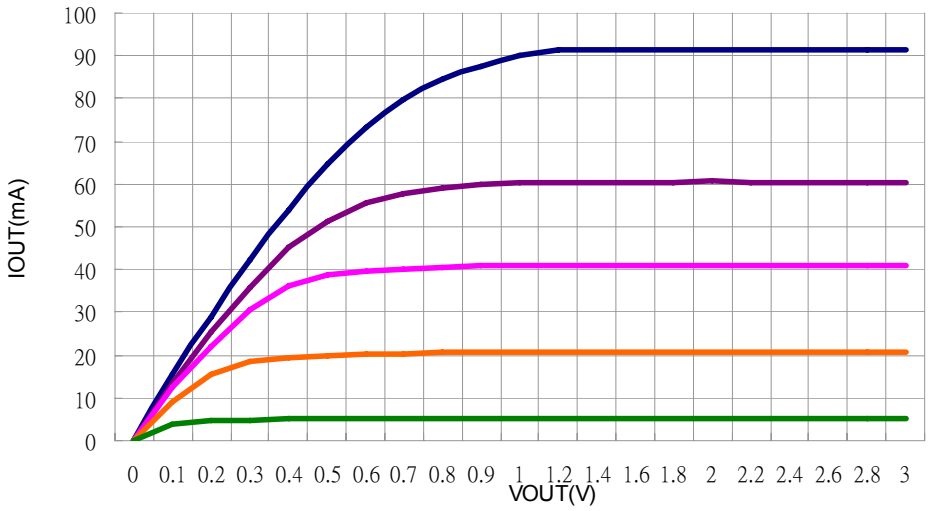


Constant-Current Output

Constant-current value of each output channel is set by an external resistor connected between the REXT pin and GND. Varying the resistor value can adjust the current scale ranging from 3mA to 90mA. The reference voltage of REXT terminal (Vrext) is approximately 1.23V. The output current value is calculated by the following equation:



In order to obtain a good performance of constant-current output, a suitable output voltage is necessary. Users can get related information about the minimum output voltage below.



Serial Data Interface

DM13H includes a flexible data transfer interface. The data can be transferred from DAI pin to the shift registers at the rising edge of CLK. After all data are clocked in, a rising edge of the $\overline{LAT}$ signal can transfer the serial data to the data latches (Edge trigger). The serial data format can be 16-bit or 10-bit wide, depending on the operating mode of the device.

Operation Mode

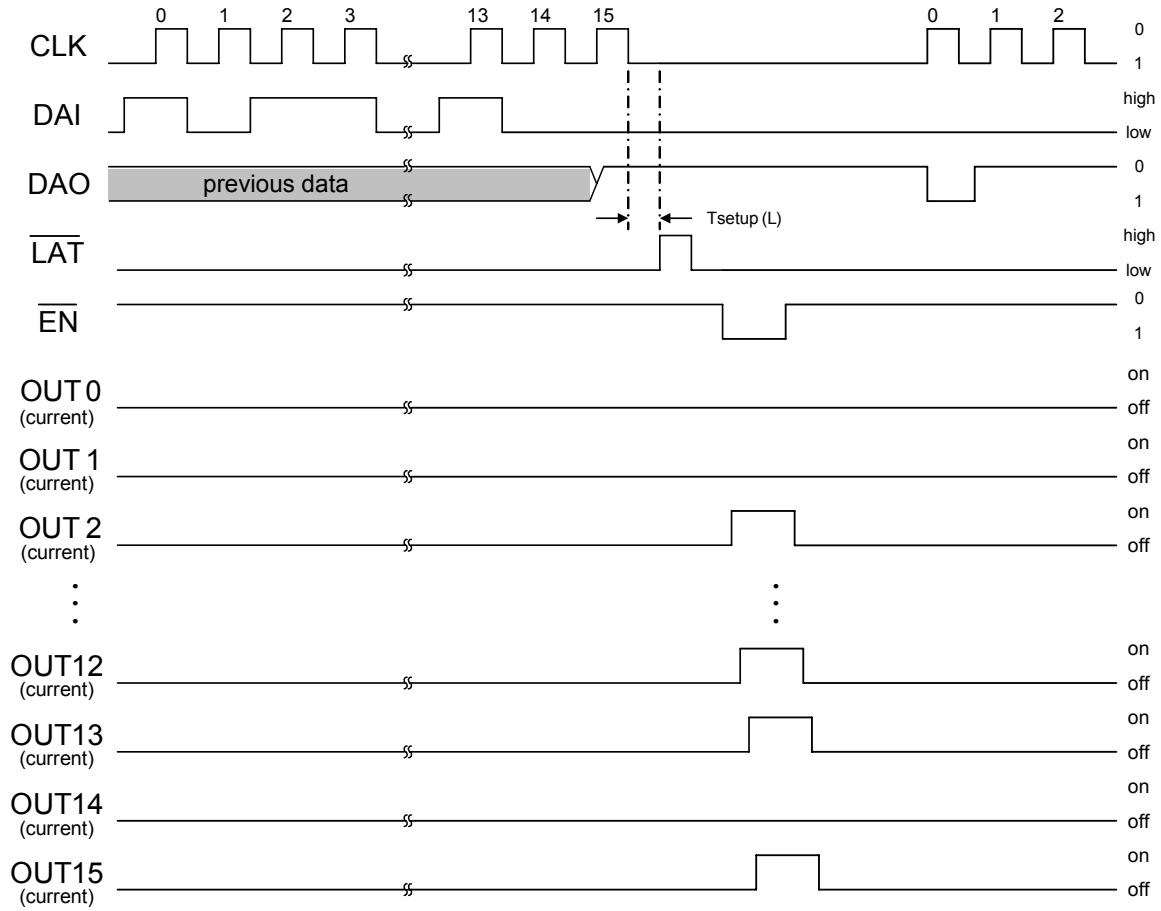
DM13H has two operating modes depending on the combination of CLK and $\overline{LAT}$ signals. The table below shows the available operating modes. For normal operation (SD mode), the data width of shift register is 16-bit, which is used to set 16 bits serial-in image data. The sequence of the combination of CLK and $\overline{LAT}$ explains in following pages is used to change the operation mode. If there are four triggering clock pulses (CLK) with high level latch ($\overline{LAT}$), DM13H will change to command data input mode (CD mode) at falling edge of the latch pulse ($\overline{LAT}$) then user can make ten triggering clock pulses to set 7-bit GBC data (default value after power-on is 7'b1000000), 1-bit voltage level selection of short detection (default value after power-on is 1'b1) and 1-bit sleep control data (default value is 1'b0)

OPERATION MODE	SHIFT REGISTER
Serial-in Data Input Mode (SD mode)	16-bit
Command Data Input Mode (CD mode)	10-bit

SD Mode Data Format

MSB 15	14	13	12	11		4	3	2	1	LSB 0
OUT15	OUT14	OUT13	OUT12	OUT11	• • •	OUT4	OUT3	OUT2	OUT1	OUT0
Shift-in first										

When DM13H operates at SD mode, the serial-in data (DAI) will be clocked into 16-bit shift register synchronized on the rising edge of the clock (CLK). The data '1' represents the corresponding current output 'ON', while the data '0' stands for 'OFF'. The data will be transferred into the 16 bit latch synchronized on the rising edge of the strobe signal ($\overline{LAT}$); otherwise, the output data won't be changed. The latch pulse should be sent after the falling edge of the last clock within a frame data.



CD Mode Data Format

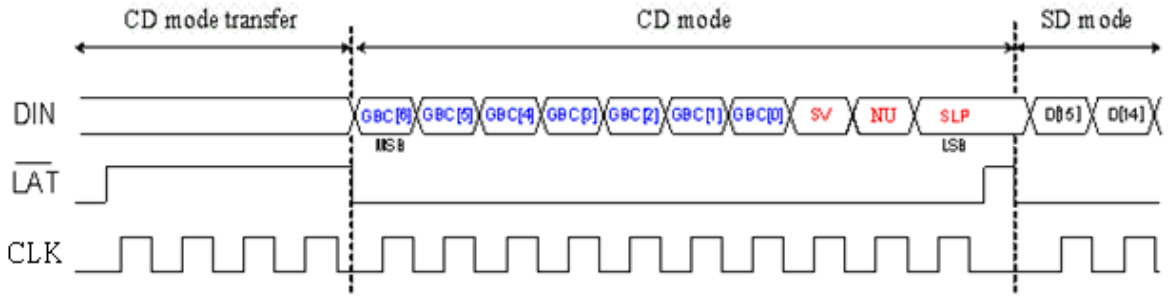
MSB 9	8	7	6	5	4	3	2	1	LSB 0
G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	SV	NU	SLP

Shift- in first

G[6:0] :Global Brightness Control SV : LED short detection Level select SLP : Sleep select
NU : "0" for normal operation

a. Global Brightness Control

DM13H offers a convenient way to fine tune the whole chip output currents for the uniformity of brightness between modules, ICs or the accomodation to ambient light. To further adjust the current level linearly, the system shall enter the CD MODE and then shift in 7-bit GBC data code through DAI pin. The MSB should be shifted-in first. Take the input code. G[6:0]= (MSB)1001011(LSB) for example. The new current is then equal to the base current multiplied by the ratio $(2^6+2^3+2^1+2^0+1)/128$. The 7-bit data won't be changed until the next new data is latched. Note that the default code 7'b1000000 exists in chip memory when power on, so the output current is equal to the half of base current.



b. Short detection voltage level selection

DM13H provides 2 voltage levels in coordination with LED short detection on system. VCC voltage level is the default value while power-on. DAO will send an error signal = H if the output voltage is greater than a respectively predetermined threshold value.

SV	Short Voltage
0	5/6 * VCC
1	VCC (default)

c. Sleep mode

When SLP=1, DM13H will enter sleep mode, all outputs turn off and the IDD of DM13H will drop down to less than 5uA. This function is especially designed for battery or solar powered system.

Error Detection

DM13H includes Real-time and Smart detection mode for LED open/short and driver outputs short to GND detection. It can be set as six types which are showing as following table.

Detection Type	Detection Operation
Real time LED Open Detection	CLK rising edge x1, with $\overline{LAT}$=H
Real time Output Short to GND Detection	CLK rising edge x2, with $\overline{LAT}$=H
Real time LED Short Detection	CLK rising edge x3, with $\overline{LAT}$=H
Smart LED Open Detection	CLK rising edge x1, with $\overline{LAT}$=H then $\overline{LAT}$ falling edge x2 with CLK=H
Smart Output Short to GND Detection	CLK rising edge x2, with $\overline{LAT}$=H then $\overline{LAT}$ falling edge x2 with CLK=H
Smart LED Short Detection	CLK rising edge x3, with $\overline{LAT}$=H then $\overline{LAT}$ falling edge x2 with CLK=H

Selection of detection types is a collocation of CLK and $\overline{LAT}$. After detection executed, the error report will be saved in the particular shift register and could be retrieved from serial-out(DAO) data.

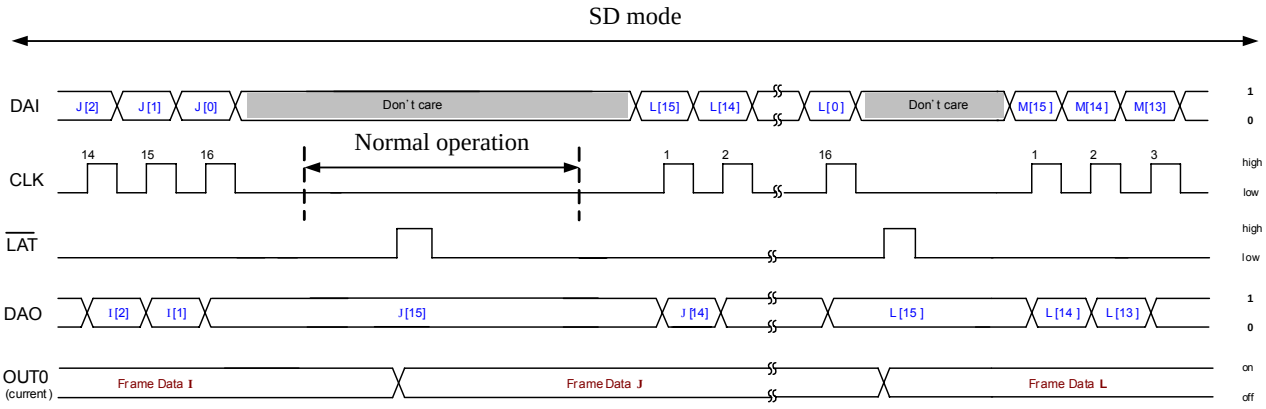
For Real-Time LED open/short detections, it's necessary to set the image data of the particular output channel as '1'. The serial-out data is '0' in the LED normal state, and the serial-out data will be '1' while a LED failure has occurred. If the image data is written to "0" or the output terminal is inactive ($\overline{EN}$=H), it will not execute any detection process for the corresponding channel. Therefore, the serial-data will remain as "0".

For Real-Time Output Short to GND detection type, set the image data of the particular output channel to '0', outputs' state will be identified from DAO as above. In output normal state, the serial-out data is '0', but if the serial-out data is '1' then a DM13H output voltage lower than 0.1V. If the image data of particular channel is '1', no detection will be executed for the corresponding channel, and the serial-out data will be '0'. Otherwise, If output enable terminal is active ($\overline{EN}$='L'), the serial-out data will be '0'.

DM13H specializes in fast detection response, 100ns minima. Moreover, it offers multi selections like ***Real-Time monitor*** and ***Smart detection***. Accordingly, it is more flexible and well adapted to the system requirements.

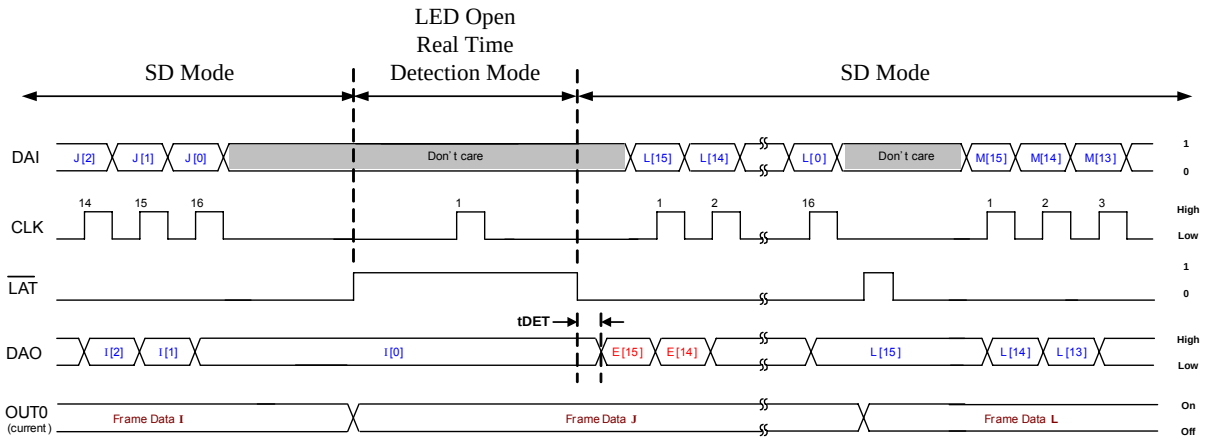
a. Normal operation

When DM13H operates at normal operation (Latch only) the DAO pin will send out the original serial-in data not the error message.

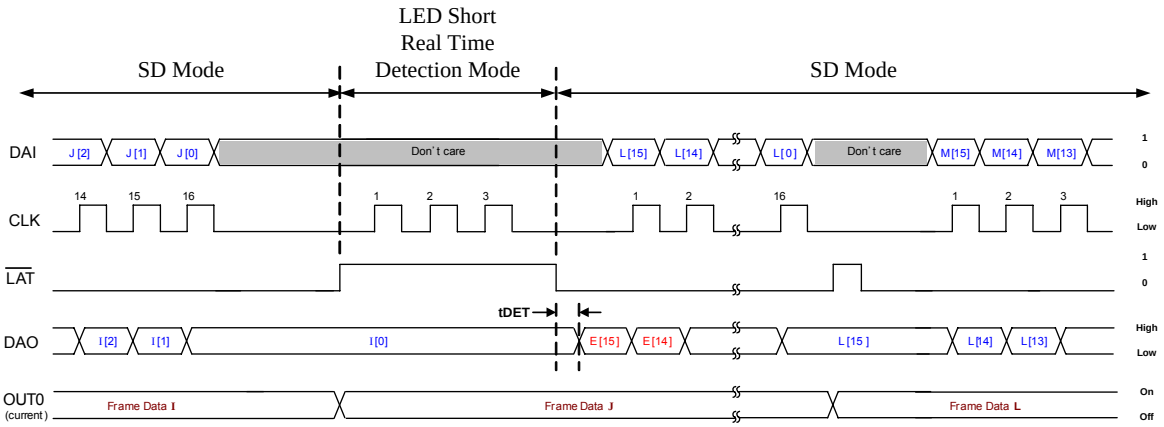


b. LED Open/Short Detection(Real-time)

Set one CLK rising edge with $\overline{LAT}$ ='H' to operate Open Real-Time detection. Each channel will be identified as a LED open failure when there is a current passing through the output but the voltage is below 0.1V.



Set three CLK rising edges with $\overline{LAT}$ ='H' to operate Short Real-Time detection. A LED short failure will be identified when the output channel is on and the output voltage is higher VCC.

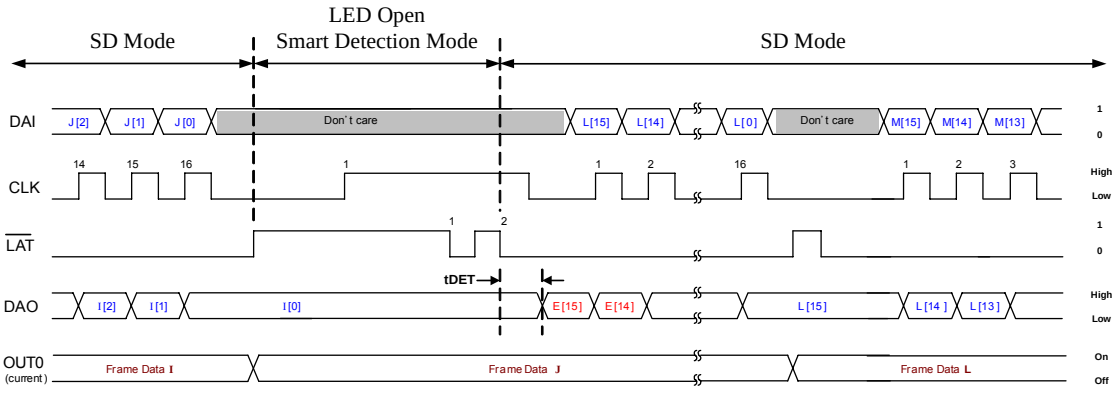


With the above operating principle, the controller could continuously retrieve LED status from serial-out(DAO) then compare with the last frame date one by one . Once there is any serial-out data at '1' be retrieved, it pinpoints the channel with failed LED. Since the process is ongoing and without shifting between image and detection mode, it does not interrupt the image data flow and the output display. This is known as "**Real-Time Monitor**".

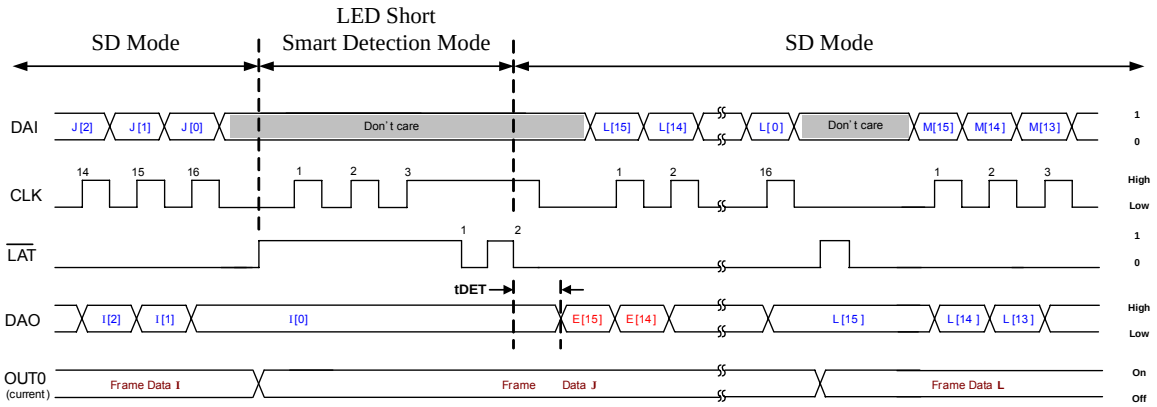
c. LED Open/Short Detection (Smart Detection)

DM13H also specially provides another **"smart"** detection method. In Smart detection mode, DM13H will automatically turns on all output channels with Iout=50uA until the next rising edge of the CLK pulse. After the rising edge of CLK, the output current will return to original state. Notice that enable control ($\overline{EN}$) won't affect smart detection result.

Set one CLK rising edge with $\overline{LAT}$ ='H' then two $\overline{LAT}$ falling edges with CLK is 'H' to operate Open Smart detection. Each channel will be identified as a LED open failure when there is a current passing through the output but the voltage is below 0.1V.



Set three CLK rising edges with $\overline{LAT}$ ='H' then two $\overline{LAT}$ falling edges with CLK is 'H' to operate Short Smart detection. A LED short failure will be identified when the output channel is off and there is a current passing through the output but the voltage is above VCC.

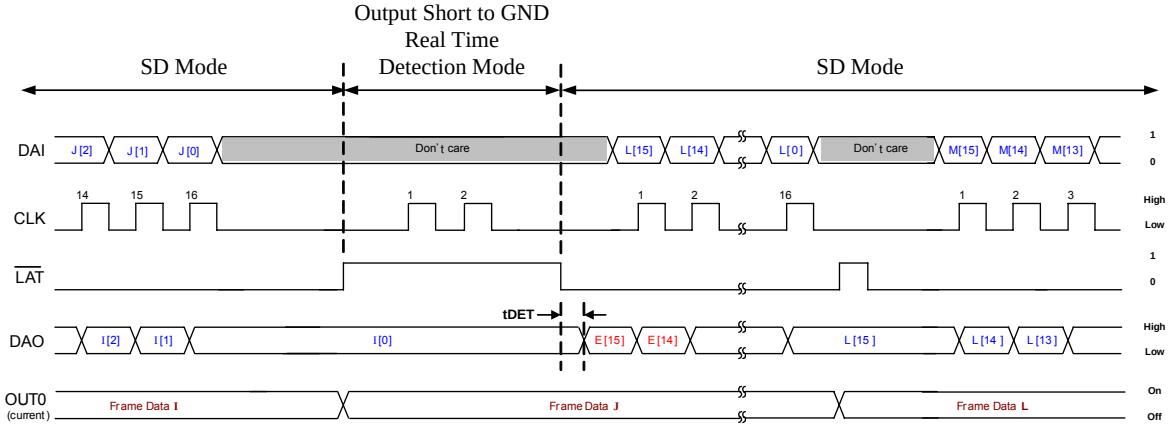


The error report of LED status will be retrieved from DAO. Once there is any serial-out data at '1' be retrieved, controller can counts clocks to identify the locations of fail LED. The impression of "**invisible failure detection**" is achievable because of less data clock-in cycle and small current during detection to avoid a flash. After Smart detection, DM13H will return to normal operation until next detection.

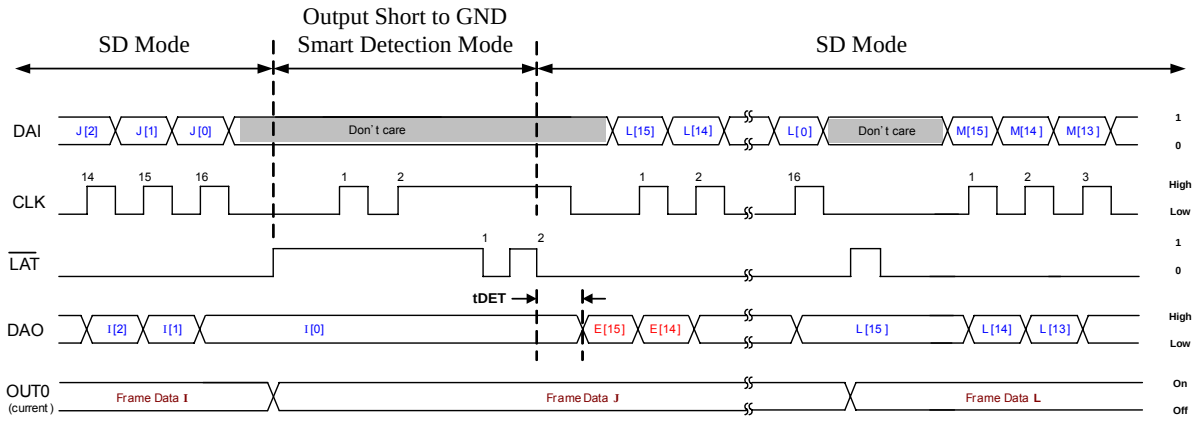
d. Outputs Short to GND Detection (Real-Time/Smart)

This error detection mode could detect the failure of IC and PCB. If IC output pins are burned-out or output pins on PCB layout are short to ground, the voltage of IC output pins would be pulled to low voltage. It will make LEDs turn on all the time. Therefore, DM13H would determine the failure of IC output pins when the output voltage is below 0.1V. For the duration of output short to GND smart detection, the output would be turned off automatically and pulled high to VDD no matter channel is on or off.

Set two CLK rising edges with $\overline{LAT}$ ='H' to operate Output Short to GND Real-Time detection. An output short failure will be identified when the output turn off but the voltage is below 0.1V.

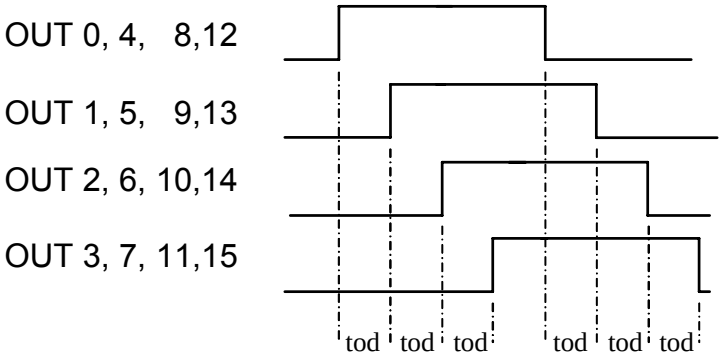


Set two CLK rising edges with $\overline{LAT}$ ='H' then sending two $\overline{LAT}$ falling edges with CLK is 'H' to operate Output Short to GND Smart detection. DM13H will force all outputs to turn off automatically, and start to detect output short error until the next rising edge of CLK pulse. After the rising edge of CLK, the output current will return to original value. After the detection, device will return to Normal Operation. Notice that enable control ($\overline{EN}$) won't affect smart detection result.



Outputs Delay

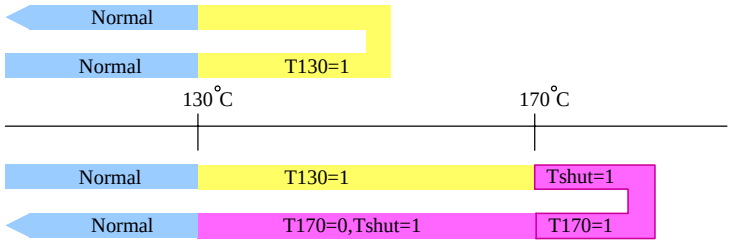
Large in-rush currents will occur when the system activates all the outputs at once. To prevent this effect, a constant unit of delay between outputs is built-in DM13H. All outputs are divided into four groups and each group contains four outputs. For example, OUT0 ~ OUT3 form the group1; OUT4 ~ OUT7 form the group2. There is no delay between every group. But each output delay between channels in a group is 3ns @VDD=3.3V (typical).



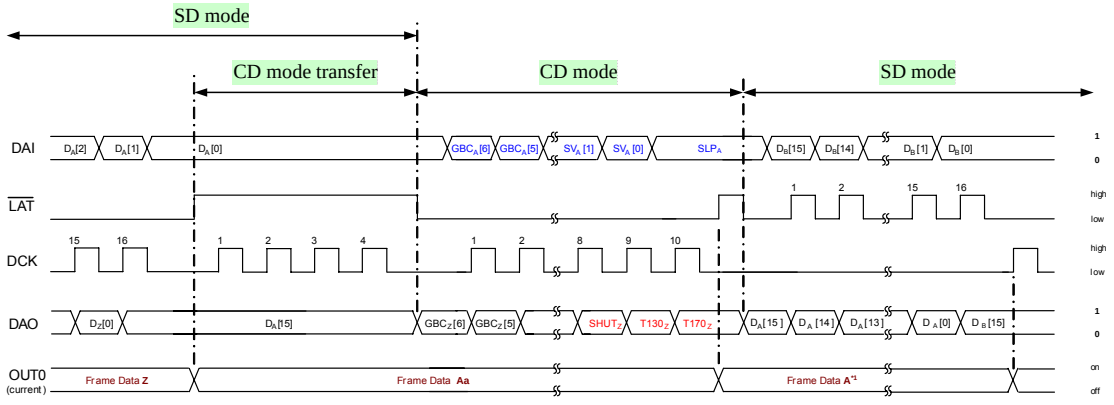
Thermal Alarm and Shutdown

DM13H provides a temperature error detection circuit for thermal alarm and shutdown protection. When junction temperature of the IC exceeds 130℃, the thermal flag(T130) will be serial-out in the CD mode. If no cooling measures to reduce the temperature(by system), the junction temperature might continue to rise. Once it reaches to 170℃, DM13H will turn off all outputs. When the junction temperature is lower than 130℃, DM13H will restart automatically. Operation in the over-temperature situation(> 130℃) for a long time may cause chip damage permanently.

Thermal Flag	Description
T130	130℃ temperature flag "H" : Temp ≧ 130℃, "L" : Temp < 130℃
T170	170℃ temperature flag "H" : Temp ≧ 170℃, "L" : Temp < 170℃
Tshut	Shutdown Flag "H" : 16 outputs off, "L" : normal operation



In CD mode, thermal flags will be serial-out through DAO. According to these thermal flags, the control system can adopt proper way to protect whole display system. Please note the thermal flags are all 'L' in normal operation.



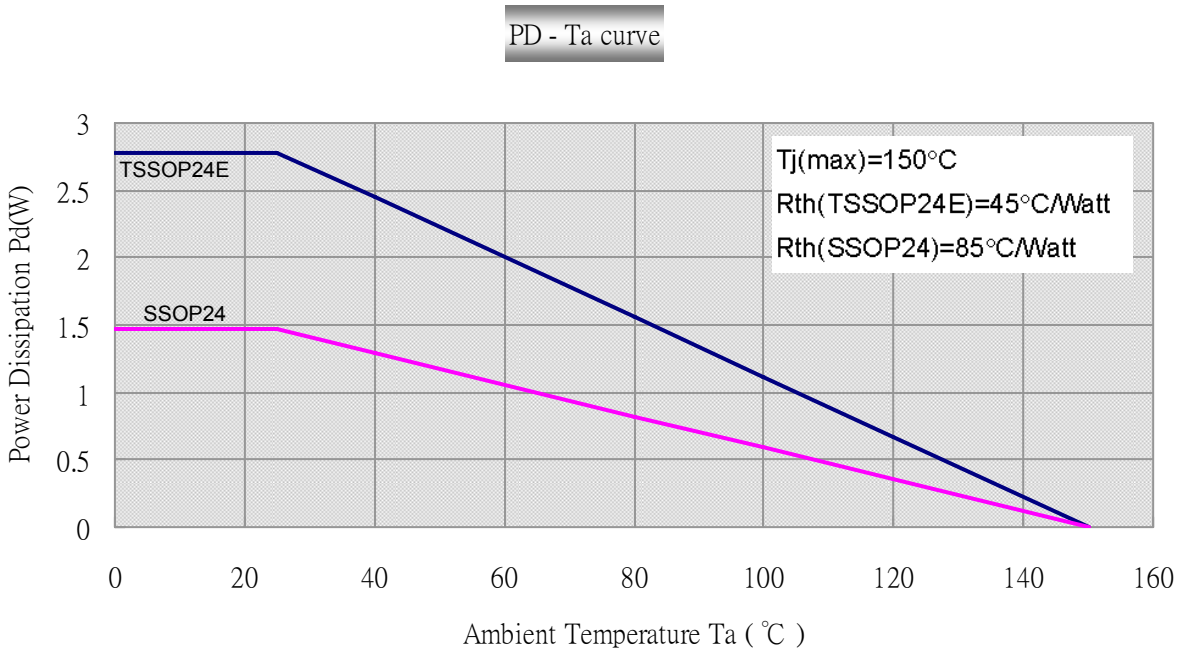
*1 The difference between Frame data A and Aa is the max output current.

Power Dissipation

Notice that the power dissipation of a semiconductor chip is limited to its package and ambient temperature, in which the device requires the maximum output current calculated for given operating conditions. The maximum allowable power consumption can be calculated by the following equation:

$$Pd(max)(Watt) = \frac{Tj(junction\ temperature)(max)(℃) - Ta(ambient\ temperature)(℃)}{Rth(junction\text{-}to\text{-}air\ thermal\ resistance)(℃/Watt)}$$

The relationship between power dissipation and operating temperature can be refer to the figure below:

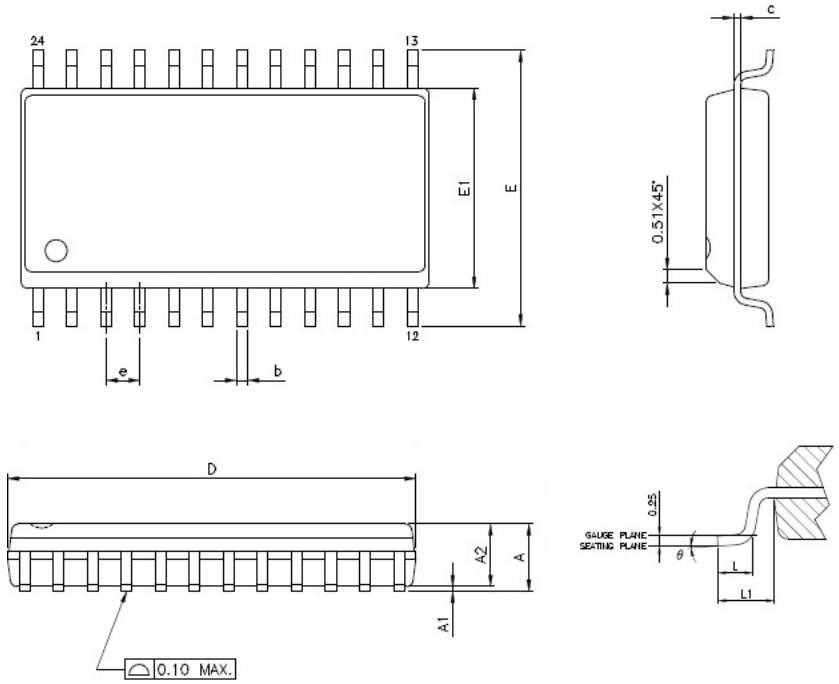


The power consumption of IC can be determined by the following equation and should be less than the maximum allowable power dissipation:

$$Pd(W) = V_{CC}(V) \times I_{DD}(A) + Vout0 \times Iout0 \times Duty0 + \cdots\cdots + Vout15 \times Iout15 \times Duty15 \leq Pd(max)(W)$$

Package Outline Dimension

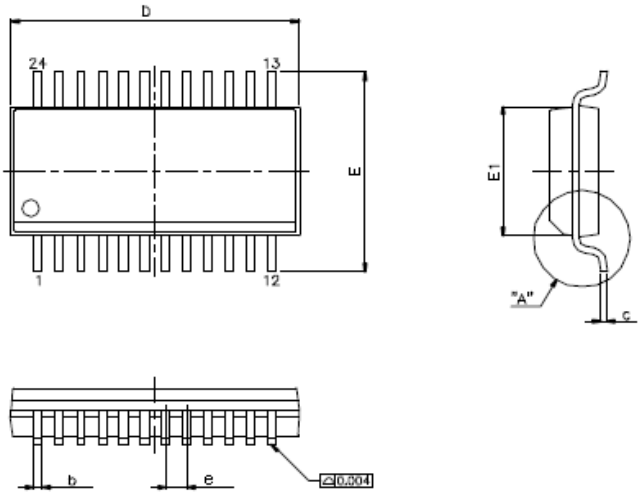
SOP24

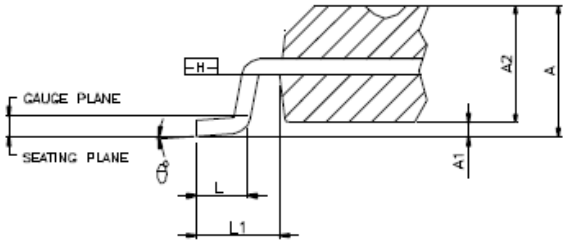


Dimensions in mm			
Symbol	MIN.	TYP.	MAX.
A	-	-	2.650
A1	0.100	-	0.300
A2	2.050	-	-
b	0.310	-	0.510
c	0.200	-	0.330
D	15.240	-	15.700
E1	7.500 BSC		
e	1.270 BSC		
E	10.300 BSC		
L1	1.40 REF		
L	0.400	-	1.270
θ°	0	-	8

Package Outline Dimension

SSOP24

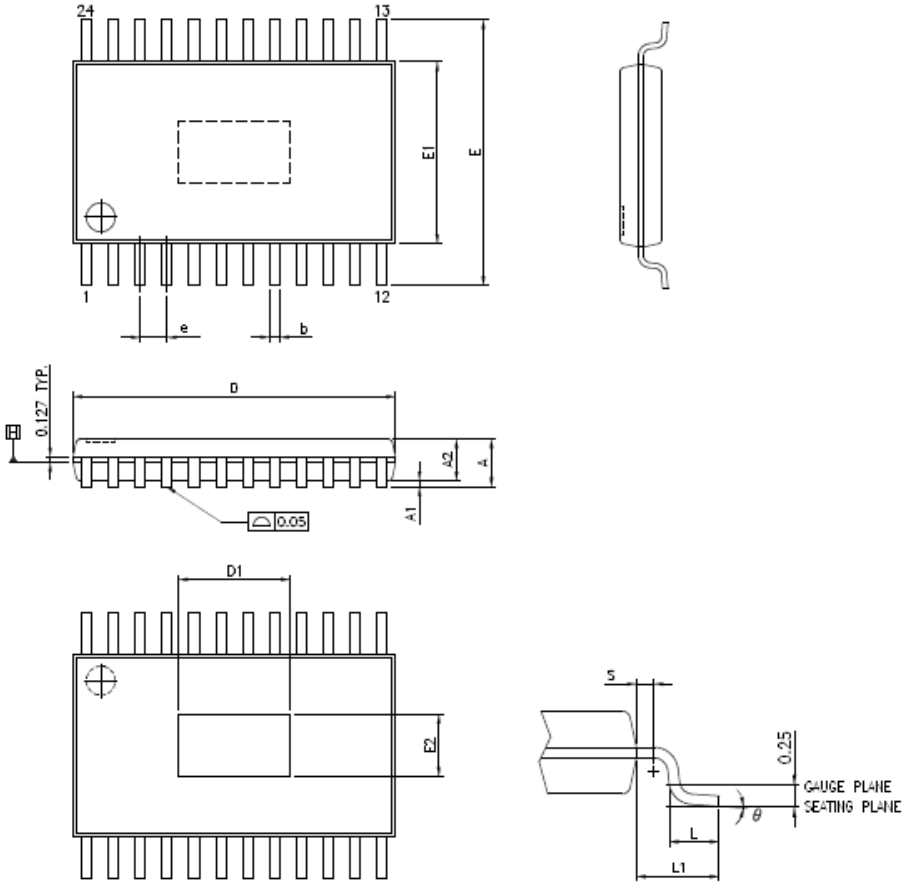




	Dimensions in inch			Dimensions in mm		
Symbol	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.01	0.102	0.152	0.254
A2	-	-	0.059	-	-	1.499
b	0.008	-	0.012	0.203	-	0.305
C	0.007	-	0.01	0.178	-	0.254
D	0.337	0.341	0.344	8.56	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
e	0.025 BSC			0.635 BSC		
E1	0.15	0.154	0.157	3.81	3.912	3.988
L	0.016	0.025	0.05	0.406	0.635	1.27
L1	0.041 BSC			1.041 BSC		
θ°	0	-	8	0	-	8

Package Outline Dimension

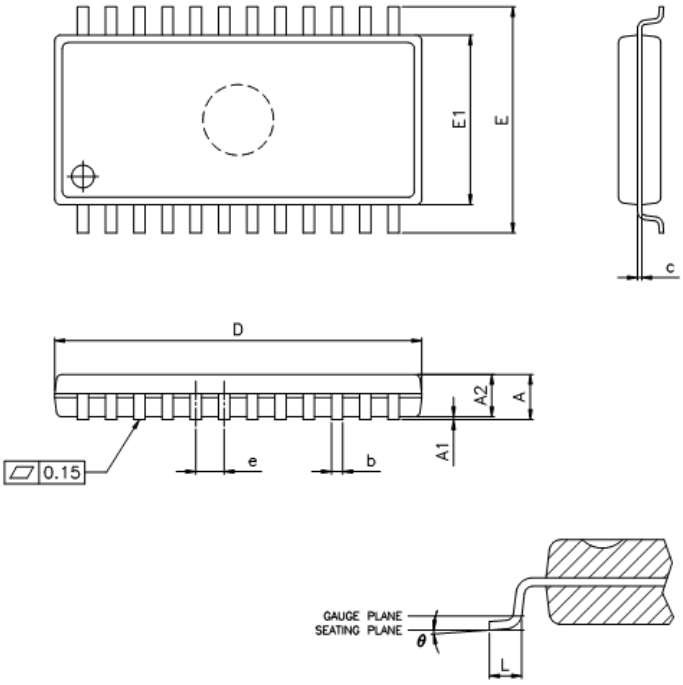
TSSOP24E



	Dimensions in inch			Dimensions in mm		
Symbol	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	-	-	0.047	-	-	1.2
A1	0	-	0.006	0	-	0.15
A2	0.031	0.039	0.041	0.8	1	1.05
b	0.007	-	0.012	0.19	-	0.3
D	0.303	7.8	0.311	7.7	7.8	7.9
E1	0.169	4.4	0.177	4.3	4.4	4.5
E	6.400 BSC			6.400 BSC		
e	0.650 BSC			0.650 BSC		
L1	1.000 REF			1.000 REF		
L	0.018	4.4	0.03	0.45	0.6	0.75
S	0.008	-	-	0.2	-	-
θ°	0	-	8	0	-	8
PAD SIZE2 (112×18E)						
E2	0.09	-	0.112	2.28	-	2.85
D1	0.146	-	0.182	3.7	-	4.62

Package Outline Dimension

SOP24B

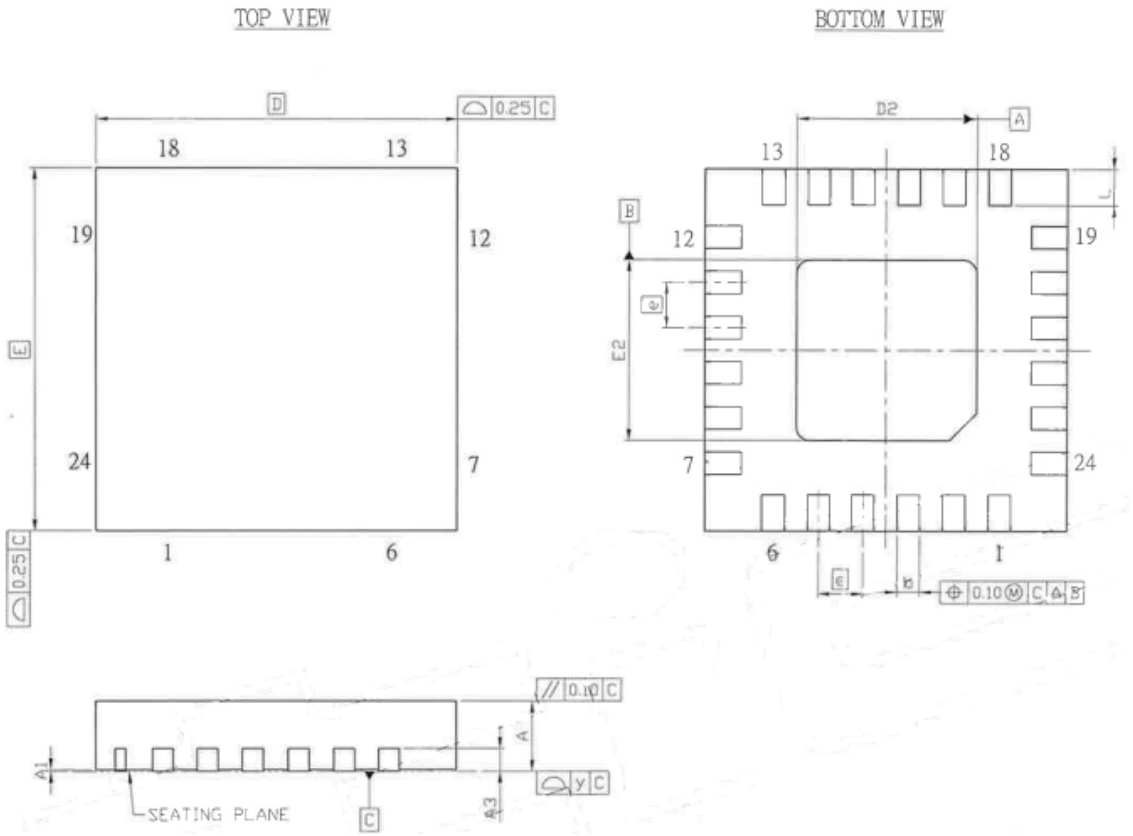


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.90
A1	0.05	0.10	0.20
A2	1.30	1.50	1.70
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	12.80	13.00	13.20
E	7.70	8.00	8.30
E1	5.80	6.00	6.20
e	1.00 BSC		
L	0.25	0.45	0.65
θ	0°	–	10°

Package Outline Dimension

QFN24



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3	0.203 REF			8 REF		
b	0.18	0.25	0.30	7.09	9.84	11.81
D	3.90	4.00	4.10	153.5	157.5	161.4
D2	1.90	2.00	2.10	74.8	78.7	82.7
E	3.90	4.00	4.10	153.5	157.5	161.4
E2	1.90	2.00	2.10	74.8	78.8	82.7
e	0.50 BSC			19.69 BSC		
L	0.30	0.40	0.50	11.8	15.7	19.7
y	0.08			3.15		

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