



TLV62095 4-A High Efficiency Step Down Converter with DCS-Control™

1 Features

- 2.5 V to 5.5 V Input Voltage Range
- DCS-Control™
- Up to 95% Efficiency
- Power Save Mode
- 20 μ A Operating Quiescent Current
- 100% Duty Cycle for Lowest Dropout
- 1.4 MHz Typical Switching Frequency
- 0.8 V to V_{IN} Adjustable Output Voltage
- Output Discharge Function
- Adjustable Soft Startup
- Hiccup Short Circuit Protection
- Output Voltage Tracking
- Pin-to-Pin Compatible with [TLV62090](#) and [TPS62095](#)
- For Improved Feature Set, See [TPS62095](#)

2 Applications

- TV, STB, Computers
- Solid State Drives (SSD)
- Hard Disk Drives (HDD)
- Battery Powered Applications

3 Description

The TLV62095 device is a high frequency synchronous step-down converter optimized for small solution size, high efficiency and suitable for battery powered applications. To maximize efficiency, the converter operates in PWM mode with a nominal switching frequency of 1.4MHz and it automatically enters Power Save Mode operation at light load currents. When used in distributed power supplies and point of load regulation, the device allows voltage tracking to other voltage rails and tolerates output capacitors ranging from 10 μ F to 150 μ F and beyond. Using the DCS-Control™ topology, the device achieves excellent load transient performance and accurate output voltage regulation.

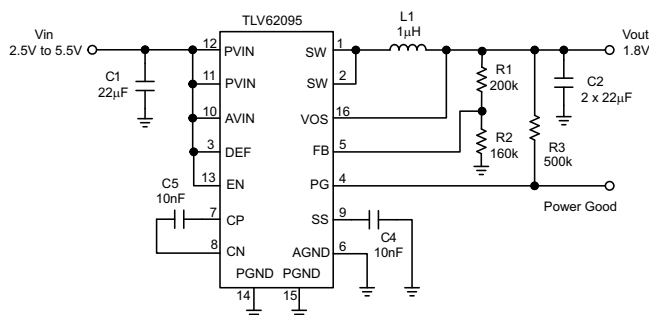
The output voltage start-up ramp is controlled by the soft startup pin, which allows operation as either a standalone power supply or in tracking configurations. Power sequencing is also possible by configuring the EN and PG pins. In Power Save Mode, the device operates with typically 20- μ A quiescent current. Power Save Mode is entered automatically and seamlessly maintaining high efficiency over the entire load current range.

The device is available in a 3 mm x 3 mm 16-pin VQFN package.

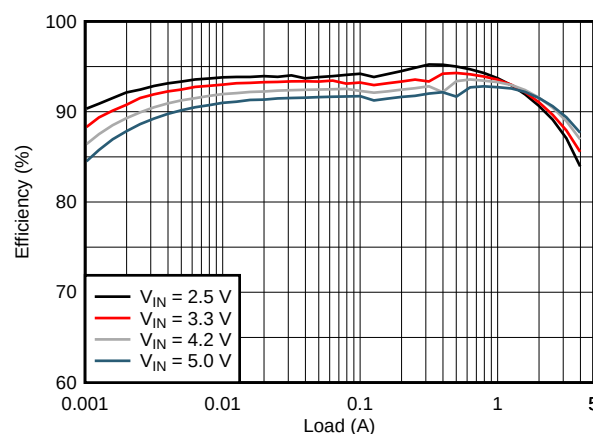
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV62095	VQFN (16)	3.00 mm x 3.00 mm

1.8 V Output Application



1.8 V Output Application Efficiency



D001



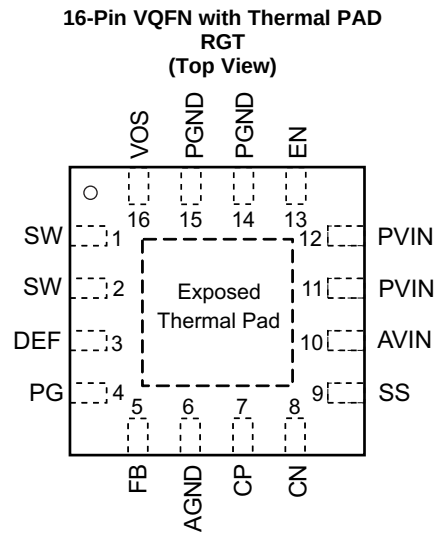
Table of Contents

1 Features	1	7.4 Device Functional Modes.....	8
2 Applications	1	8 Application and Implementation	11
3 Description	1	8.1 Application Information.....	11
4 Revision History	2	8.2 Typical Applications	11
5 Pin Configuration and Functions	3	9 Power Supply Recommendations	16
6 Specifications	4	10 Layout	16
6.1 Absolute Maximum Ratings	4	10.1 Layout Guidelines	16
6.2 Handling Ratings.....	4	10.2 Layout Example	17
6.3 Recommend Operating Conditions.....	4	10.3 Thermal Consideration.....	17
6.4 Thermal Information	4	11 Device and Documentation Support	18
6.5 Electrical Characteristics.....	5	11.1 Device Support.....	18
6.6 Typical Characteristics	6	11.2 Community Resources.....	18
7 Detailed Description	7	11.3 Trademarks	18
7.1 Overview	7	11.4 Electrostatic Discharge Caution.....	18
7.2 Functional Block Diagram	7	11.5 Glossary	18
7.3 Feature Description.....	8	12 Mechanical, Packaging, and Orderable Information	18

4 Revision History

DATE	REVISION	NOTES
March 2016	*	Initial release.

5 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
SW	1, 2	Switch pin of the power stage.
DEF	3	This pin is used for internal logic and needs to be pulled high. This pin must be connected to the AVIN pin.
PG	4	Power good open drain output. A pull up resistor can not be connected to any voltage higher than the input voltage.
FB	5	Feedback pin for regulating the output voltage.
AGND	6	Analog ground.
CP	7	Internal charge pump's flying capacitor. Connect a 10nF capacitor between CP and CN.
CN	8	Internal charge pump's flying capacitor. Connect a 10nF capacitor between CP and CN.
SS	9	Soft-start control pin. A capacitor is connected to this pin and sets the soft startup time. Leaving this pin floating sets the minimum start-up time.
AVIN	10	Analog supply input voltage pin.
PVIN	11,12	Power supply input voltage pin.
EN	13	Enable pin. This pin has an active pull down resistor of typically 400kΩ, which is active when EN is low. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device.
PGND	14,15	Power ground.
VOS	16	Output voltage sense pin. This pin must be directly connected to the output voltage.
Exposed Thermal Pad		The exposed thermal pad must be connected to AGND. It must be soldered for mechanical reliability.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

		MIN	MAX	UNIT
Voltage at pins ⁽²⁾	PVIN, AVIN, FB, SS, EN, DEF, VOS	–0.3	7.0	V
	SW, PG	–0.3	V _{IN} +0.3	
	CN, CP	–0.3	V _{IN} +7.0	
Sink current	PG		1.0	mA
Operating junction temperature range, T _J		–40	150	°C
Storage temperature, T _{stg}		–65	150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground pin.

6.2 Handling Ratings

			MAX	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommend Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
V _{IN}	Input voltage range	2.5	5.5	V
T _J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV62095	UNIT
		VQFN (16 PINS)	
R _{θJA}	Junction-to-ambient thermal resistance	47	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	60	
R _{θJB}	Junction-to-board thermal resistance	20	
ψ _{JT}	Junction-to-top characterization parameter	1.5	
ψ _{JB}	Junction-to-board characterization parameter	20	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	5.3	

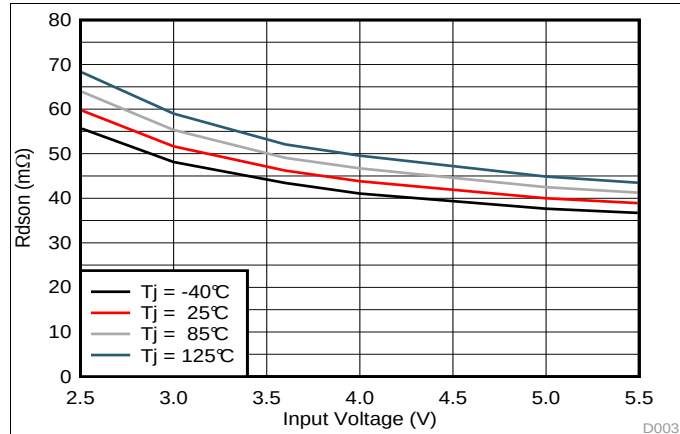
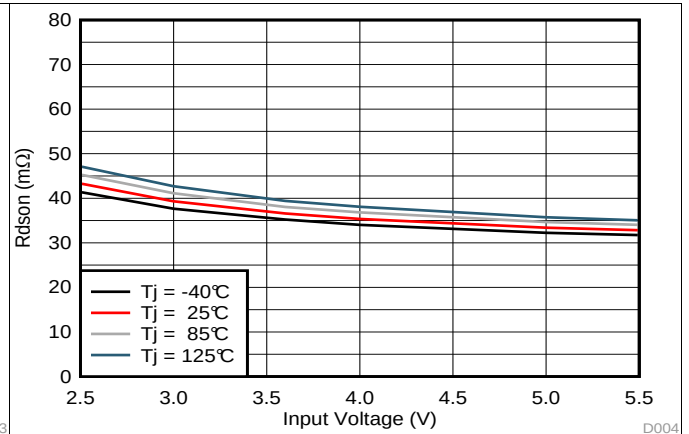
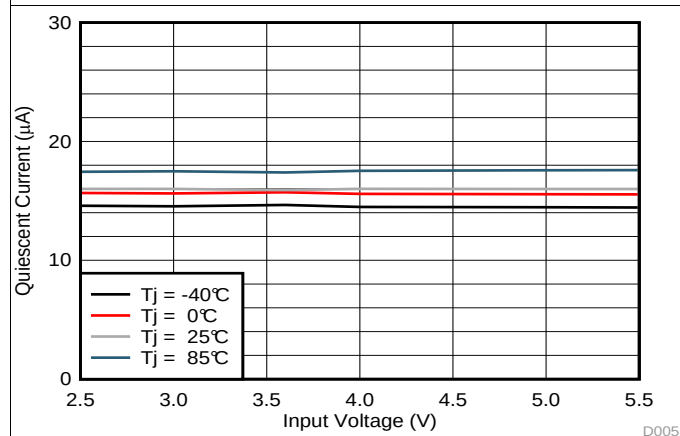
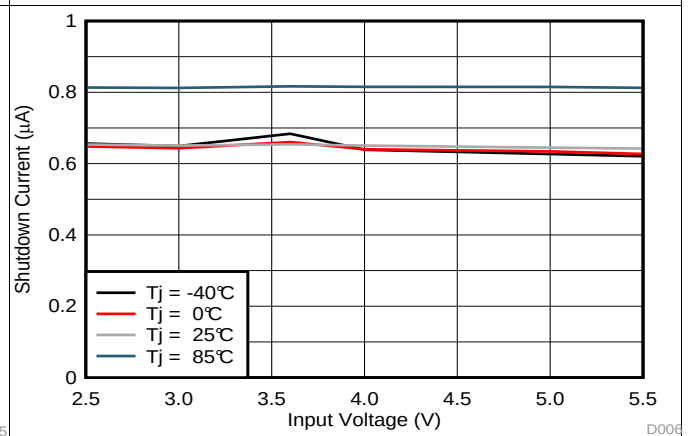
- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#)

6.5 Electrical Characteristics

 $V_{IN} = 3.6V$ and $T_J = 25^{\circ}C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		5.5	V
I_Q	Quiescent current into PVIN and AVIN	EN = High, Not switching, FB = FB +5%		20		μA
I_{SD}	Shutdown current into PVIN and AVIN	EN = Low		0.6		μA
UVLO	Undervoltage lockout threshold	V_{IN} falling	2.1	2.2	2.3	V
	Undervoltage lockout hysteresis			200		mV
	Thermal shutdown	Temperature rising		150		$^{\circ}C$
	Thermal shutdown hysteresis			20		$^{\circ}C$
CONTROL SIGNAL EN						
V_H	High level input voltage	$V_{IN} = 2.5 V$ to $5.5 V$	1	0.65		V
V_L	Low level input voltage	$V_{IN} = 2.5 V$ to $5.5 V$		0.60	0.4	V
I_{lk}	Input leakage current	EN = GND or V_{IN}		10	100	nA
R_{PD}	Pull down resistance	EN = Low		400		k Ω
SOFT STARTUP						
I_{SS}	Softstart current			7.5		μA
POWER GOOD						
V_{th}	Power good threshold	Output voltage rising		95%		V
		Output voltage falling		90%		
V_L	Low level voltage	$I_{(sink)} = 1 mA$			0.4	V
POWER SWITCH						
$R_{DS(on)}$	High side FET on-resistance	$I_{SW} = 500 mA$		50		m Ω
	Low side FET on-resistance	$I_{SW} = 500 mA$		40		m Ω
I_{LIM}	High side FET switch current limit		4.7	5.5		A
f_{SW}	Switching frequency	$I_{OUT} = 3 A$		1.4		MHz
OUTPUT						
V_{OUT}	Output voltage range		0.8		V_{IN}	V
R_{DIS}	Output discharge resistor	EN = GND, $V_{OUT} = 1.8 V$		200		Ω
V_{FB}	Feedback regulation voltage	$I_{OUT} = 1 A$, PWM mode	792	800	808	mV
	Line regulation	$V_{OUT} = 1.8 V$, PWM operation		0.016		%/V
	Load regulation	$V_{OUT} = 1.8 V$, PWM operation		0.04		%/A

6.6 Typical Characteristics


Figure 1. High-Side FET On Resistance

Figure 2. Low-Side FET On Resistance

Figure 3. Quiescent Current

Figure 4. Shutdown Current

7.3 Feature Description

7.3.1 PWM Operation

At medium to heavy load currents, the device operates with pulse width modulation (PWM) at a nominal switching frequency of 1.4 MHz. As the load current decreases, the converter enters power save mode operation reducing its switching frequency. The device enters power save mode at the boundary to discontinuous conduction mode (DCM).

7.3.2 Power Save Mode Operation

As the load current decreases, the converter enters Power Save Mode operation. During Power Save Mode, the converter operates with reduced switching frequency to maintain high efficiency. Power Save Mode is based on a fixed on-time architecture following [Equation 1](#).

$$t_{on} = \frac{V_{OUT}}{V_{IN}} \times 360ns \times 2$$

$$f = \frac{2 \times I_{OUT}}{t_{on}^2 \left(1 + \frac{V_{IN} - V_{OUT}}{V_{OUT}} \right) \times \frac{V_{IN} - V_{OUT}}{L}} \quad (1)$$

In Power Save Mode, the output voltage rises slightly above the nominal output voltage in PWM mode. This effect is reduced by increasing the output capacitance or the inductor value. This effect is also reduced by programming the output voltage of the TLV62095 lower than the target value.

7.3.3 Low Dropout Operation (100% Duty Cycle)

The device offers low input to output voltage difference by entering 100% duty cycle mode. In this mode the high side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage where the output voltage falls below its set point is given by:

$$V_{IN(min)} = V_{OUT} + I_{OUT} \times (R_{DS(on)} + R_L) \quad (2)$$

Where

$R_{DS(on)}$ = High side FET on-resistance

R_L = DC resistance of the inductor

7.4 Device Functional Modes

7.4.1 Enable (EN)

The device is enabled by setting the EN pin to a logic high. Accordingly, shutdown mode is forced if the EN pin is pulled low with a shutdown current of typically 0.6 μ A. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal resistor of 200 Ω discharges the output through the VOS pin smoothly. An internal pull-down resistor of 400 k Ω is connected to the EN pin when the EN pin is low. The pull-down resistor is disconnected when the EN pin is high.

7.4.2 Soft Startup (SS) and Hiccup Current Limit During Startup

To minimize inrush current during startup, the device has an adjustable startup time depending on the capacitor value connected to the SS pin. The device charges the SS capacitor with a constant current of typically 7.5 μ A. The feedback voltage follows this voltage divided by 1.56, until the internal reference voltage of 0.8 V is reached. The soft startup operation is completed once the voltage at the SS capacitor has reached typically 1.25 V. The soft startup time is calculated using [Equation 3](#). The larger the SS capacitor, the longer the soft startup time. The relation between the SS pin voltage and the FB pin voltage is estimated using [Equation 4](#).

$$t_{SS} = C_{SS} \times \frac{1.25V}{7.5\mu A} \quad (3)$$

$$V_{FB} = \frac{V_{SS}}{1.56} \quad (4)$$

Device Functional Modes (continued)

During startup the switch current limit is reduced to 1/3 of its typical current limit of 5.5A when the output voltage is less than 0.6V. Once the output voltage exceeds typically 0.6V, the switch current limit is released to its nominal value. Thus, the device provides a reduced load current of 1.8A when the output voltage is below 0.6V. Due to this, a small or no startup time may trigger this reduced switch current limit during startup, especially for larger output capacitor applications. This is avoided by using a larger soft start up capacitance which extends the soft startup time. See [Short Circuit Protection \(Hiccup-Mode\)](#) for details of the reduced current limit during startup. Leaving the SS pin floating sets the minimum startup time (around 50 μ s).

7.4.3 Voltage Tracking (SS)

The SS pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in [Figure 5](#). The internal reference voltage follows the voltage at the SS pin with a fraction of 1.56 until the internal reference voltage of 0.8 V is reached. The device achieves ratiometric or coincidental (simultaneous) output tracking, as shown in [Figure 6](#).

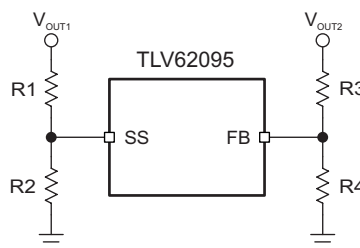


Figure 5. Output Voltage Tracking

The R2 value should be set properly to achieve accurate voltage tracking by taking 7.5 μ A soft startup current into account. 1 k Ω or smaller is a sufficient value for R2.

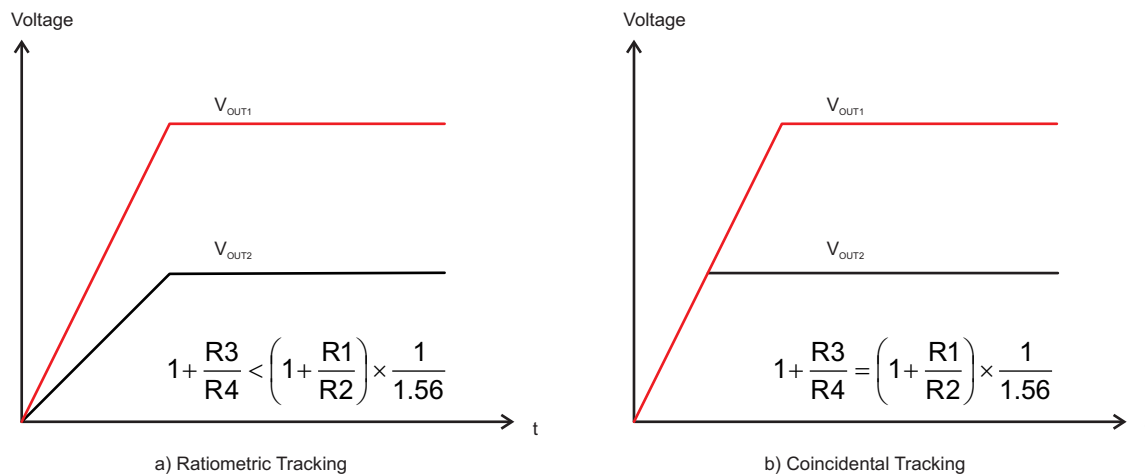


Figure 6. Voltage Tracking Options

For decreasing the SS pin voltage, the device doesn't sink current from the output when the device is in power save mode. So the resulting decrease of the output voltage may be slower than the SS pin voltage if the load is light. When driving the SS pin with an external voltage, do not exceed the voltage rating of the SS pin which is 7 V.

Device Functional Modes (continued)

7.4.4 Short Circuit Protection (Hiccup-Mode)

The device is protected against hard short circuits to GND and over-current events. This is implemented by a two level short circuit protection. During start-up and when the output is shorted to GND, the switch current limit is reduced to 1/3 of its typical current limit of 5.5 A. Once the output voltage exceeds typically 0.6 V the current limit is released to its nominal value. The full current limit is implemented as a hiccup current limit. Once the internal current limit is triggered 32 times, the device stops switching and starts a new start-up sequence after a typical delay time of 66 μ s passed by. The device repeats these cycles until the high current condition is released.

7.4.5 Output Discharge Function

To make sure the device starts up under defined conditions, the output gets discharged via the VOS pin with a typical discharge resistor of 200 Ω whenever the device shuts down. This happens when the device is disabled or if thermal shutdown, undervoltage lockout or short circuit hiccup-mode is triggered.

7.4.6 Power Good Output

The power good output is low when the output voltage is below its nominal value. The power good becomes high impedance once the output is within 5% of regulation. The PG pin is an open drain output and is specified to sink up to 1mA. This output requires a pull-up resistor to be monitored properly. The pull-up resistor cannot be connected to any voltage higher than the input voltage of the device. The PG output is low when the device is disabled in thermal shutdown or UVLO. The PG output can be left floating if unused.

7.4.7 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. UVLO shuts down the device at input voltages lower than typically 2.2 V with a 200 mV hysteresis.

7.4.8 Thermal Shutdown

The device goes into thermal shutdown once the junction temperature exceeds typically 150°C with a 20°C hysteresis.

7.4.9 Charge Pump (CP, CN)

The CP and CN pins must attach to an external 10 nF capacitor to complete a charge pump for the gate driver. This capacitor must be rated for the input voltage. It is not recommended to connect any other circuits to the CP or CN pins.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV62095 is a 4-A high frequency synchronous step-down converter optimized for small solution size, high efficiency and suitable for battery powered applications.

8.2 Typical Applications

8.2.1 1.8-V Output Converter

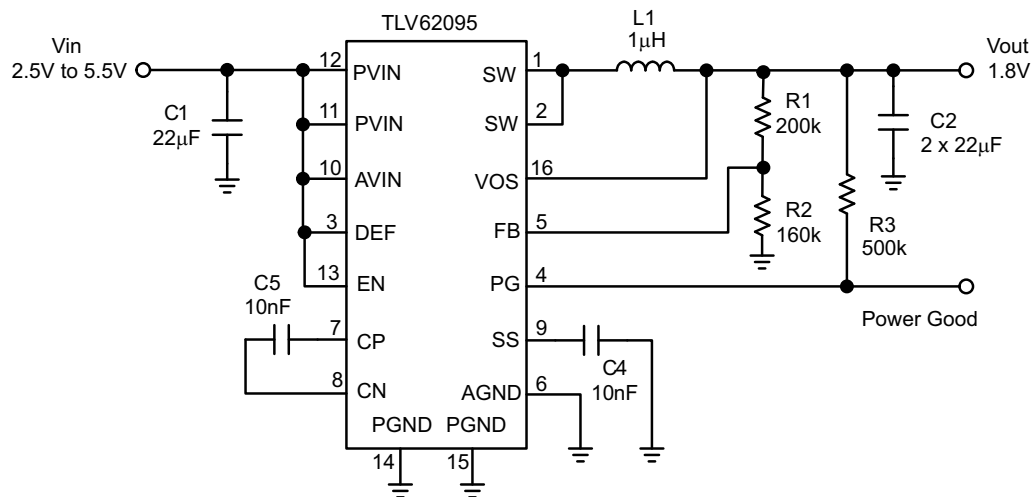


Figure 7. TLV62095 Typical Application Circuit

8.2.1.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating conditions. For the typical application example, the following input parameters are used.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 5.5 V
Output voltage	1.8 V
Output ripple voltage	< 30 mV
Output current rating	4 A

Table 2 shows the list of components for the Application Characteristic Curves.

Table 2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
TLV62095	High efficiency step-down converter	Texas Instruments
L1	Inductor: 1 µH	Coilcraft XAL4020-102
C1, C2	Ceramic capacitor: 22 µF	(6.3V, X5R, 0805)

Table 2. List of Components (continued)

REFERENCE	DESCRIPTION	MANUFACTURER
C4, C5	Ceramic capacitor, 10 nF	Standard
R1, R2, R3	Resistor	Standard

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Output Filter

The first step is the selection of the output filter components. To simplify this process, [Table 3](#) outlines possible inductor and capacitor value combinations.

Table 3. Output Filter Selection

INDUCTOR VALUE [μH] ⁽¹⁾	OUTPUT CAPACITOR VALUE [μF] ⁽²⁾				
	10	22	2 x 22	100	150
0.47					
1.0			√ ⁽³⁾	√	√
2.2					

- (1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
- (2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%.
- (3) Typical application configuration. Other check mark indicates alternative filter combinations

8.2.1.2.2 Inductor Selection

The inductor selection is affected by several parameters like inductor ripple current, output voltage ripple, transition point into Power Save Mode, and efficiency. See [Table 4](#) for typical inductors.

Table 4. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER ⁽¹⁾	SIZE (LxWxH mm)	Isat / DCR
1 μH	Coilcraft XAL4020-102	4.0 x 4.0 x 2.1	8.75A / 13.2 mΩ
0.47 μH	TOKO DFE322512C	3.2 x 2.5 x 1.2	5.9A / 21 mΩ

(1) See [Third-Party Products](#) disclaimer

In addition, the inductor has to be rated for the appropriate saturation current and DC resistance (DCR). The inductor needs to be rated for a saturation current as high as the typical switch current limit of 5.5A or according to [Equation 5](#) and [Equation 6](#). [Equation 5](#) and [Equation 6](#) calculate the maximum inductor current under static load conditions. The formula takes the converter efficiency into account. The converter efficiency can be taken from the data sheet graphs or 80% can be used as a conservative approach. The calculation must be done for the maximum input voltage where the peak switch current is highest.

$$I_L = I_{OUT} + \frac{\Delta I_L}{2} \quad (5)$$

$$I_L = I_{OUT} + \frac{\frac{V_{OUT}}{\eta} \times \left(1 - \frac{V_{OUT}}{V_{IN} \times \eta}\right)}{2 \times f \times L} \quad (6)$$

where

f = Converter switching frequency (typically 1.4MHz)

L = Inductor value

η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as a conservative assumption)

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current. A margin of 20% should be added to cover for load transients during operation.

8.2.1.2.3 Input and Output Capacitor Selection

For best output and input voltage filtering, low ESR (X5R or X7R) ceramic capacitors are recommended. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 22-μF or larger input capacitor is recommended. The output capacitor value can range from 10 μF up to 150 μF and beyond. Load transient testing and measuring the bode plot are good ways to verify stability with larger capacitor values.

The recommended typical output capacitor value is 2 x 22 μF (nominal) and can vary over a wide range as outline in the output filter selection table. Ceramic capacitor have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating.

8.2.1.2.4 Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equations:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8 \text{ V} \times \left(1 + \frac{R1}{R2}\right) \quad (7)$$

$$R2 = \frac{V_{FB}}{I_{FB}} = \frac{0.8 \text{ V}}{5 \text{ μA}} \approx 160 \text{ k}\Omega \quad (8)$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.8 \text{ V}} - 1\right) \quad (9)$$

When sizing R2, in order to achieve low quiescent current and acceptable noise sensitivity, use a minimum of 5 μA for the feedback current I_{FB} . Larger currents through R2 improve noise sensitivity and output voltage accuracy.

8.2.1.3 Application Performance Curves

$T_A = 25^\circ\text{C}$, $V_{IN} = 3.6\text{ V}$, $V_{OUT} = 1.8\text{ V}$, unless otherwise noted.

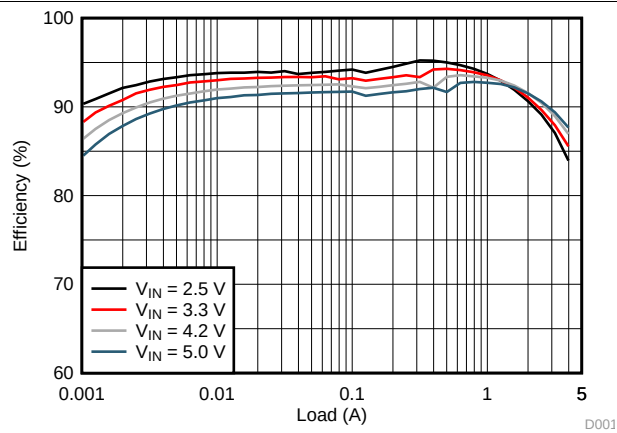


Figure 8. Efficiency, $V_{OUT} = 1.8\text{ V}$

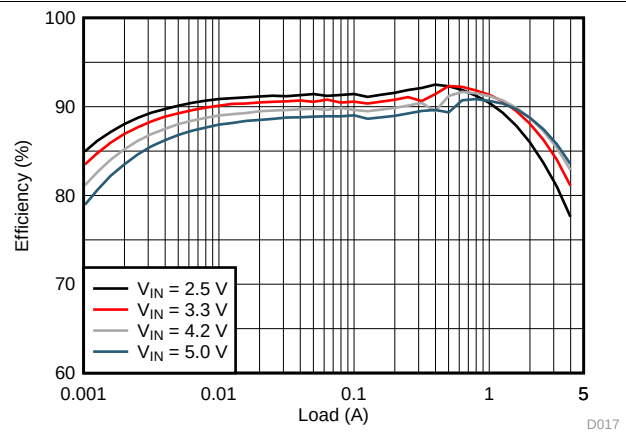


Figure 9. Efficiency, $V_{OUT} = 1.2\text{ V}$

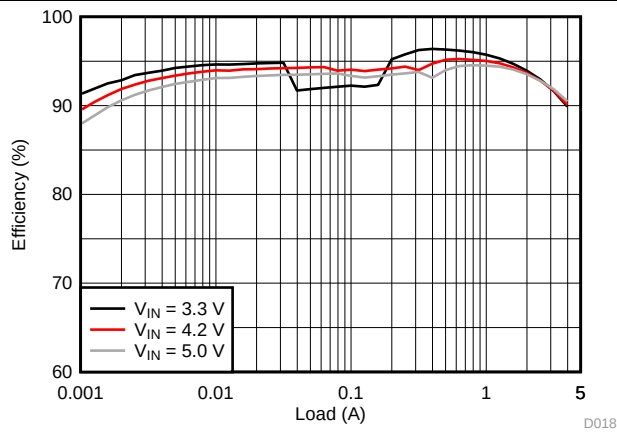


Figure 10. Efficiency, $V_{OUT} = 2.6\text{ V}$

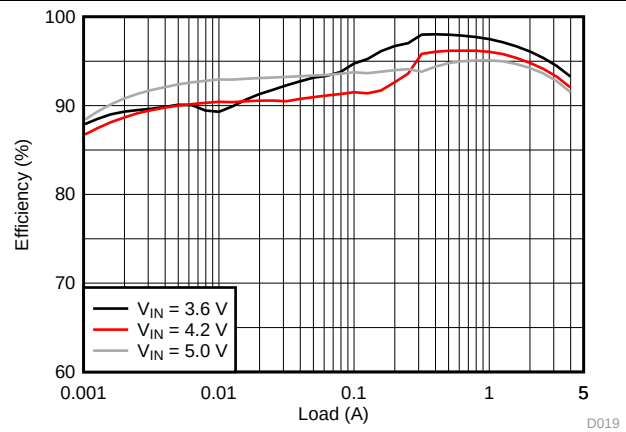


Figure 11. Efficiency, $V_{OUT} = 3.3\text{ V}$

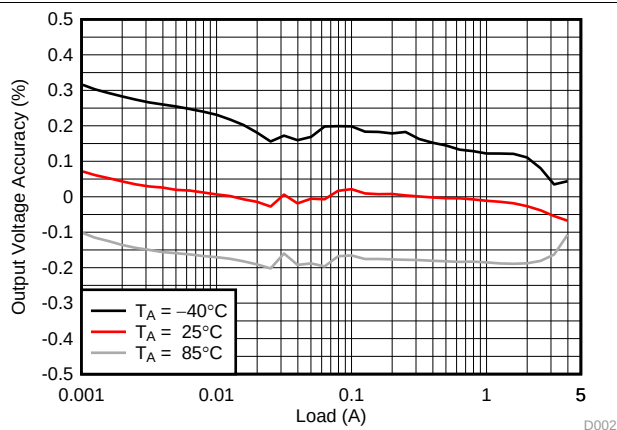


Figure 12. Load Regulation, $V_{OUT} = 1.8\text{ V}$, $V_{IN} = 3.3\text{ V}$

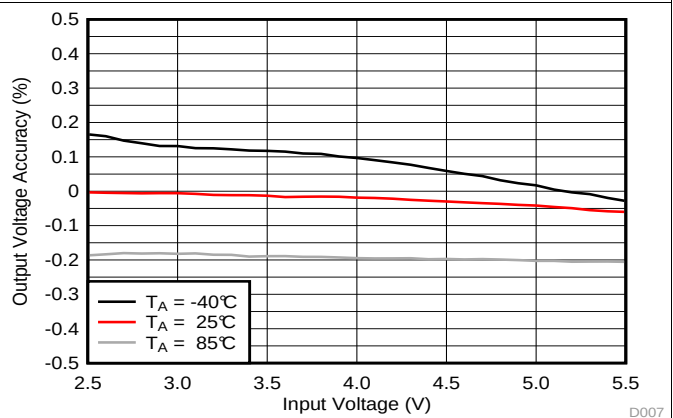


Figure 13. Line Regulation, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 1.0\text{ A}$

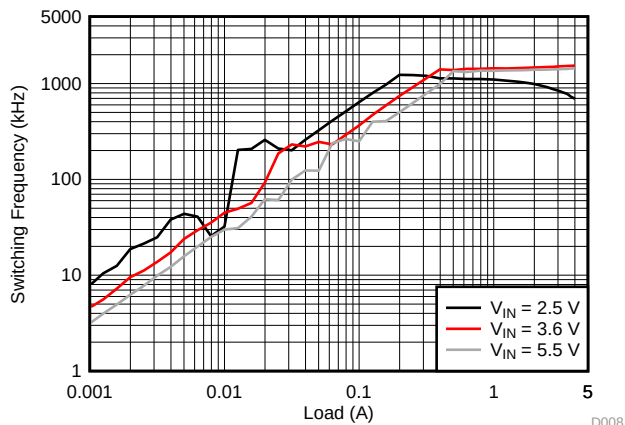


Figure 14. Switching Frequency, $V_{OUT} = 1.8\text{ V}$

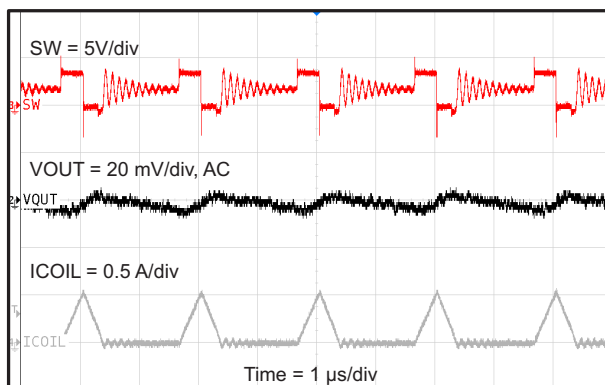


Figure 15. Output Ripple, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 100\text{ mA}$

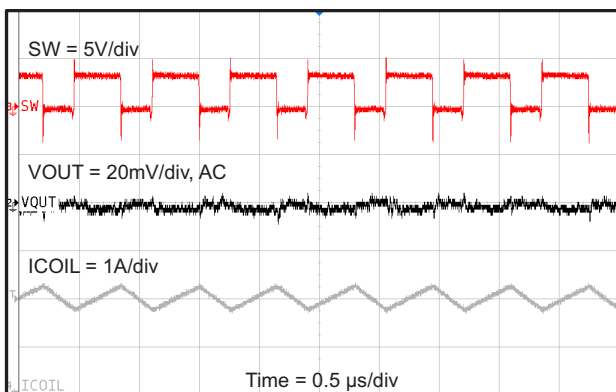


Figure 16. Output Ripple, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 3.5\text{ A}$

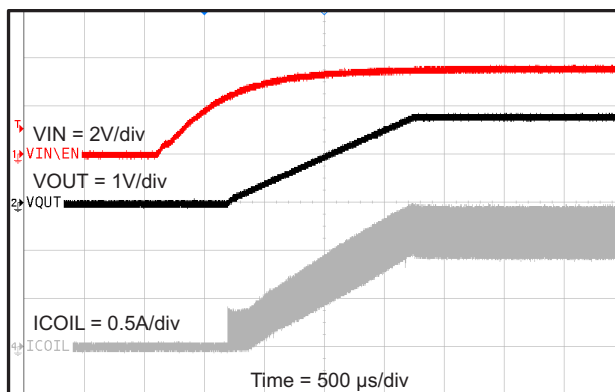


Figure 17. Startup, Relative to V_{IN} , $R_{LOAD} = 1.5\ \Omega$

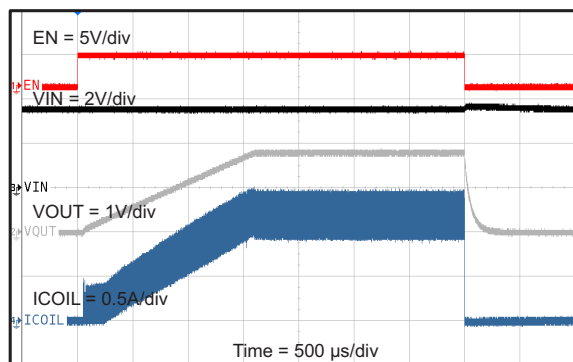


Figure 18. Startup, Relative to EN , $R_{LOAD} = 1.5\ \Omega$

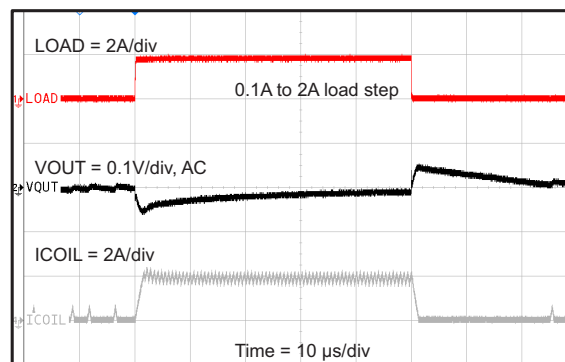
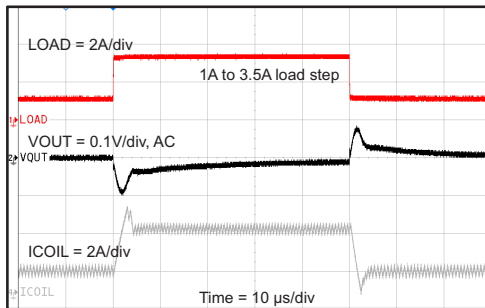
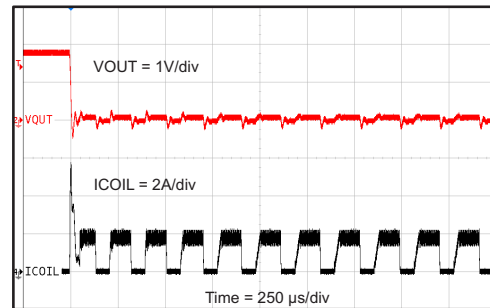
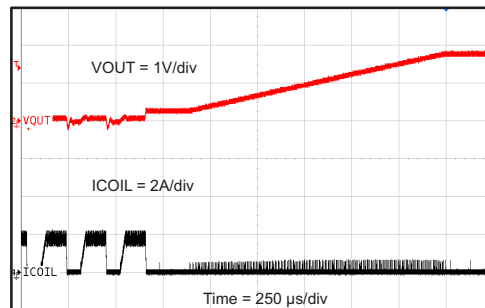


Figure 19. Load Transient, $V_{OUT} = 1.8\text{ V}$


Figure 20. Load Transient, $V_{OUT} = 1.8\text{ V}$

Figure 21. Short Circuit, HICCUP Protection Entry

Figure 22. Short Circuit, HICCUP Protection Exit

9 Power Supply Recommendations

The TLV62095 device has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TLV62095.

10 Layout

10.1 Layout Guidelines

- It is recommended to place the input capacitor as close as possible to the IC pins PVIN and PGND.
- The VOS connection is noise sensitive and needs to be routed short and direct to the output terminal of the inductor.
- The exposed thermal pad of the package, analog ground (pin 6) and power ground (pin 14, 15) should have a single point connection at the exposed thermal pad of the package. This minimizes switch node jitter.
- The charge pump capacitor connected to CP and CN should be placed close to the IC to minimize coupling of switching waveforms into other traces and circuits.
- Refer to [Figure 23](#) for an example of component placement, routing and thermal design.

10.2 Layout Example

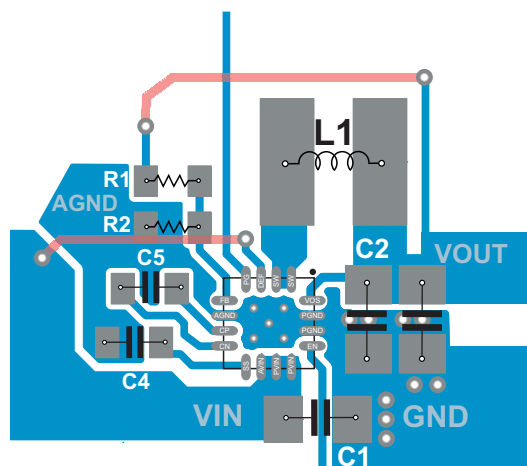


Figure 23. TLV62095 PCB Layout

10.3 Thermal Consideration

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component. The Thermal Information table provides the thermal metric of the device and its package based on JEDEC standard. For more details on how to use the thermal parameters in real applications, see the application notes: [SZZA017](#) and [SPRA953](#).

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Community Resources

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62095RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13O	Samples
TLV62095RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13O	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

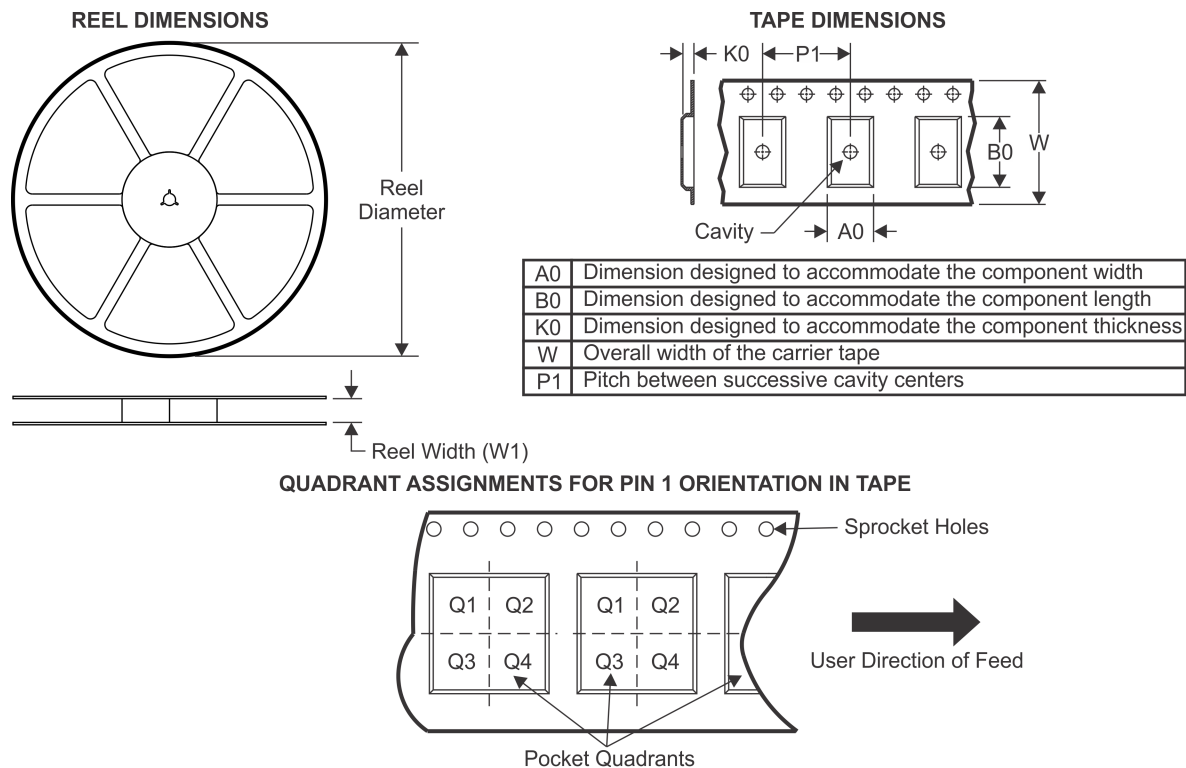
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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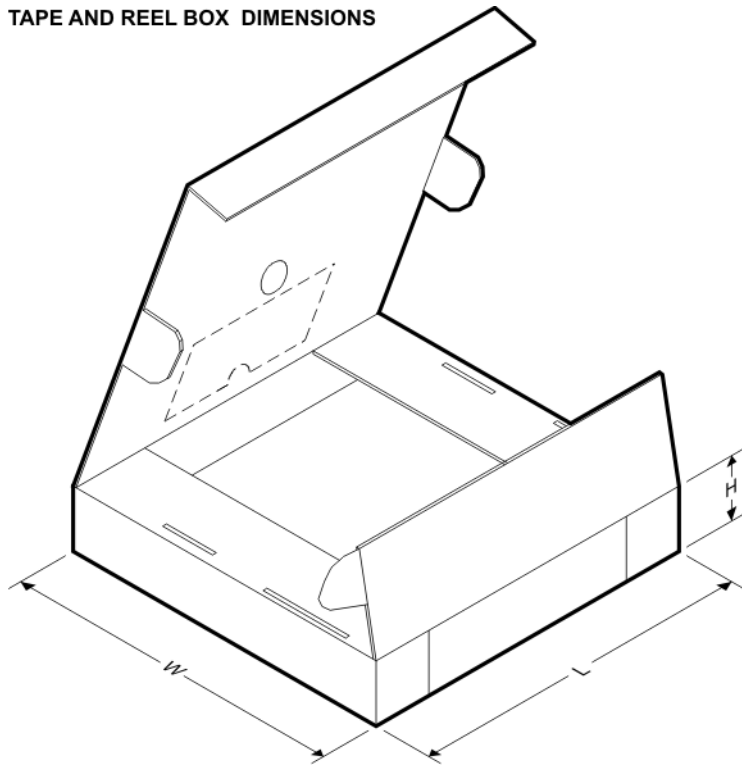
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62095RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62095RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

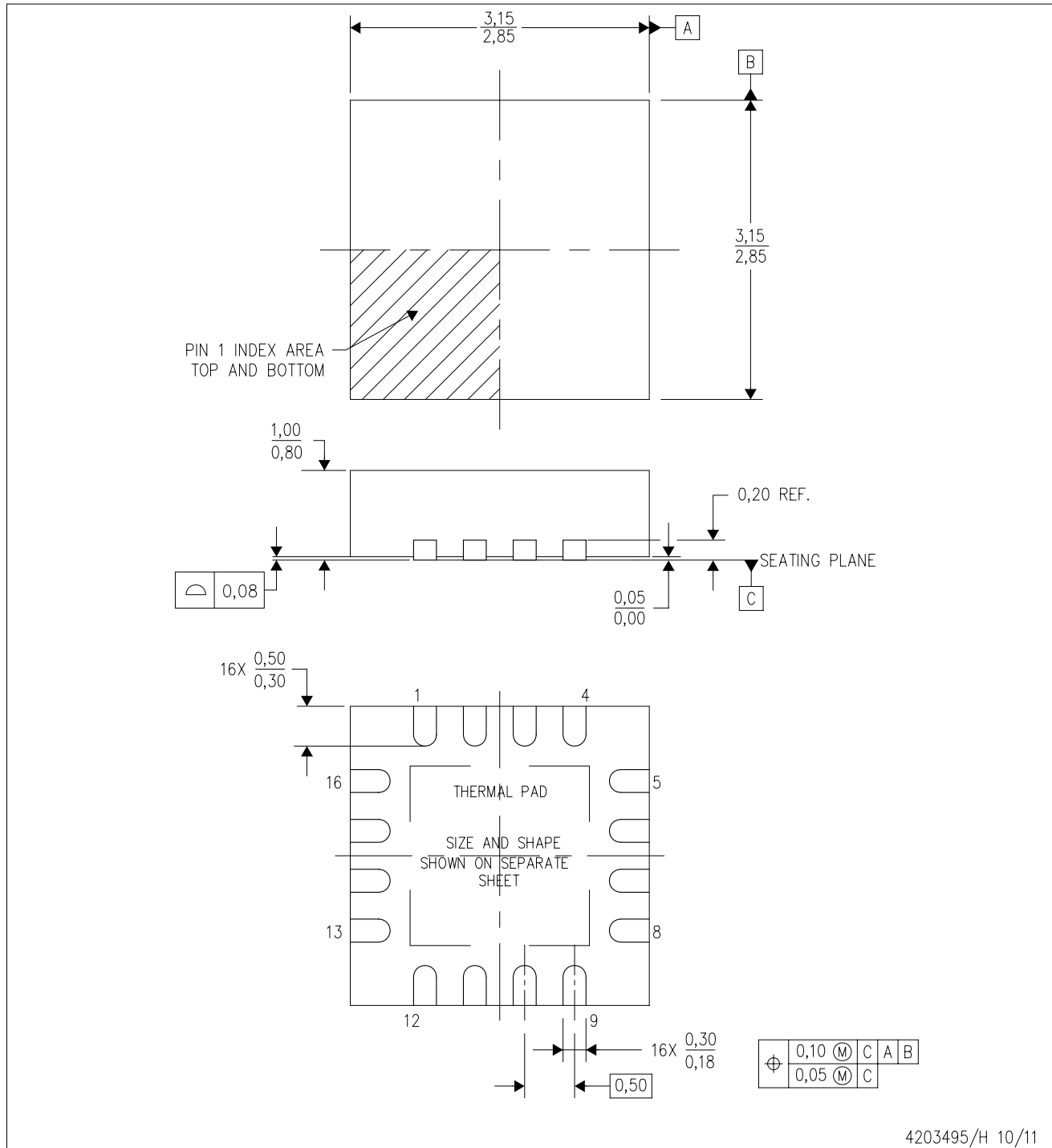


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62095RGTR	QFN	RGT	16	3000	552.0	367.0	36.0
TLV62095RGTT	QFN	RGT	16	250	552.0	185.0	36.0

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGT (S-PVQFN-N16)

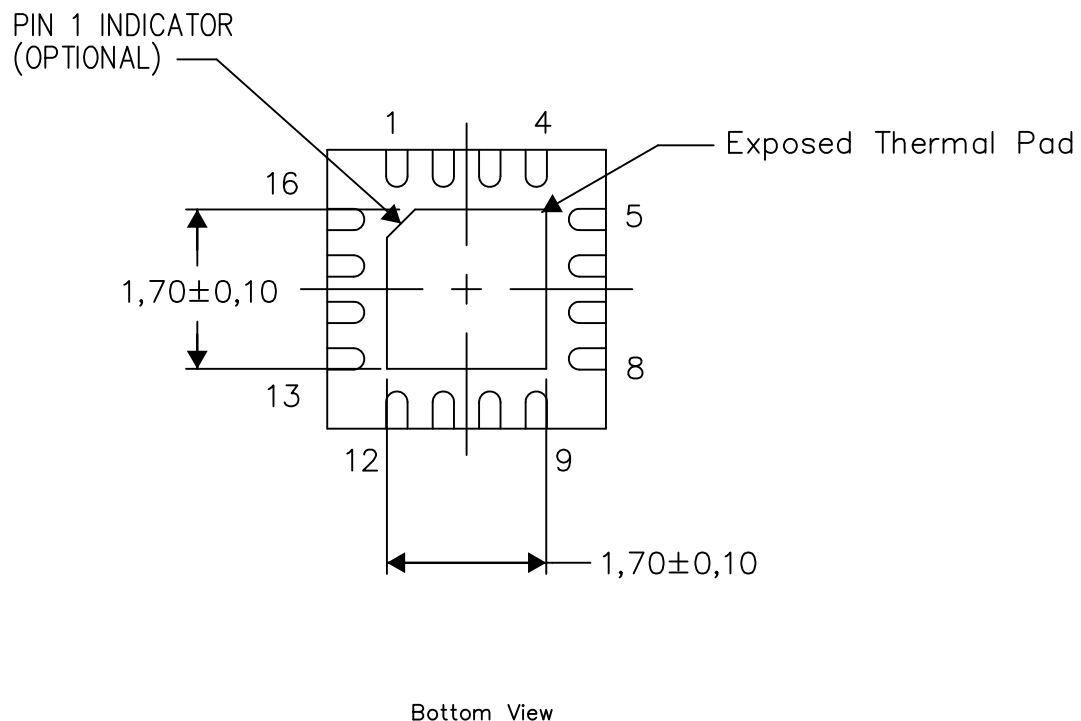
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



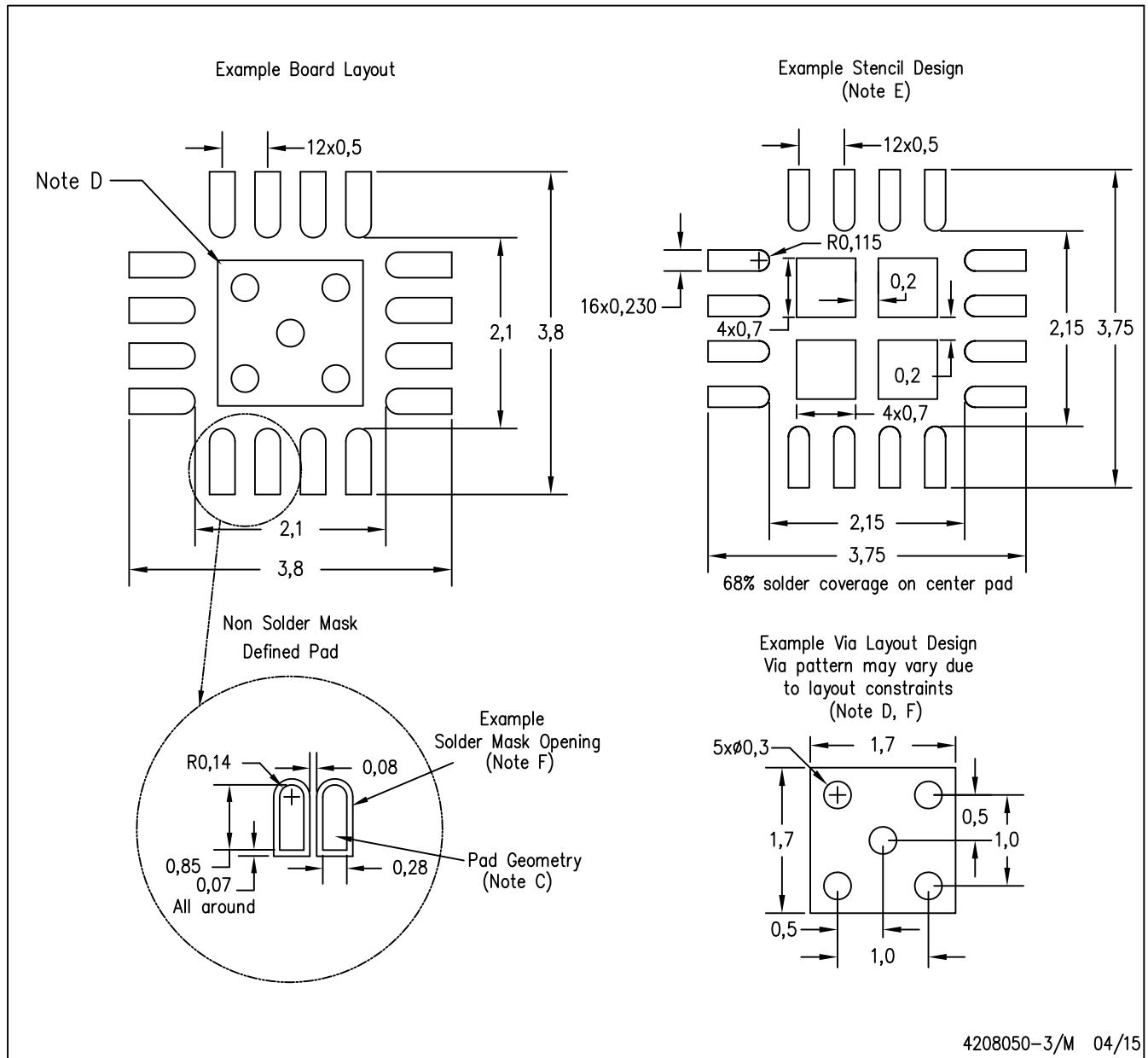
Exposed Thermal Pad Dimensions

4206349-4/Z 08/15

NOTE: All linear dimensions are in millimeters

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208050-3/M 04/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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